

**ECE 574: Modeling and synthesis of digital systems using Verilog and VHDL
Fall Semester 2009**

**Design of a VGA Display with Serial Interface
Report and Signoff due Week 7 (October 22nd)**

Design a VGA Display and Serial Interface to run on the Nexys2 board.

Characters sent over an RS232 Interface should be displayed on a 640 by 480 VGA monitor.

Part 1:

- Create a UART on the FPGA - use 19200 baud
 - Use a shift register or State Machine to create and implement your own simple receive-only UART (do not use an existing UART from picoblaze for example).
- Display the ASCII value of the received characters in hex on two of the seven-segment displays – for example “J” = 4A

Part 2:

- Create a VGA display using the VGA controller provided by Digilent (just the 640 by 480 version) – see information at end of this doc.
- Use the DIP switches to display the following patterns
 - Complete red display
 - Solid blue box 200 high by 300 wide centered in the middle of the screen.
 - A black screen with a green rectangle around the outside (one pixel wide)

(These should be relatively easy once you start working with the VGA controller provided by Digilent)

- The whole screen filled with a single character “Z” in a single color.
 - (use a constant array of 16 rows by 8 bits to define the character font and connect the 8-bits to a shift register)
 - allow for inter-character spacing on your font

(This is a bit more challenging – you will need to use the HCOUNT and VCOUNT signals to read the array and load the shift register at the correct times)

Part 3:

- Send the first three characters of your first name in upper case to the FPGA UART on the serial interface – for example “JIM”
- As the characters are received display them on the screen in the upper left corner
 - Create constant arrays for the three characters – for example ‘J’, ‘I’, ‘M’
 - Use internal FPGA memory to create a frame buffer that stores the pointer to the character to be displayed.

(This is the most challenging part of the project)

As usual, this is not a complete description – make whatever additions or changes you think are necessary.

You need to include a package in your design with a few constants defined.

Prepare a sign-off sheet and demo your system and write your report before the deadline.

Reference Material

Read the *VGA Port* section in the Nexys2 Reference Manual.

Download the VGA Component Reference Design from Digilent:

<http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,451&Prod=NEXYS2>

Make sure you read the *VGA Component Reference Design* doc in this download.

You will just need to use the ‘vga_controller_640_60.vhd file’:

```
-----  
-- vga_controller_640_60.vhd  
-----  
-- Author : Ulrich Zoltán  
--         Copyright 2006 Digilent, Inc.  
-----  
-- Software version : Xilinx ISE 7.1.04i  
--                   WebPack  
-- Device           : 3s200ft256-4  
-----  
-- This file contains the logic to generate the synchronization signals,  
-- horizontal and vertical pixel counter and video disable signal  
-- for the 640x480@60Hz resolution.  
-----  
-- Behavioral description  
-----  
-- Please read the following article on the web regarding the  
-- vga video timings:  
-- http://www.epanorama.net/documents/pc/vga_timing.html  
-----  
-- This module generates the video synch pulses for the monitor to  
-- enter 640x480@60Hz resolution state. It also provides horizontal  
-- and vertical counters for the currently displayed pixel and a blank  
-- signal that is active when the pixel is not inside the visible screen  
-- and the color outputs should be reset to 0.
```