

## **VHDL (and Verilog) for Logic Synthesis**

### **Ten simple rules!**

1. VHDL is not a programming language - an FPGA or CPLD does not execute VHDL
2. VHDL is used to describe the required behavior – necessary logic is inferred from your description
3. Always check inferred logic – verify flip-flop count - if you get latches you have done something wrong
4. Start with something simple – use multiple components
5. Where have my signals or ports gone? – synthesis tools will remove unnecessary logic and ports
6. Synthesis tools may correct simple errors
7. A simulator executes your VHDL without change
8. VHDL may simulate OK but fail to produce correct hardware
9. Make a test bench as soon as possible
10. Don't try and hack your way to a solution – start again!