Lab 1: Combinational Logic Design
Demo and signoff due during first week of labs

Lab exercise 1: (worth 5% of total lab grade)

This lab is to remind you how to use the Xilinx Vivado Design Suite tools and the Basys3 (or older Nexys3 board) board to implement a combinational logic design.

Background Review

Complete the Decoder tutorial (in Verilog) - you may find it helpful to also look at the Counter tutorial showing how to instantiate a lower level module.

Description

Part 1:

• Create a new module called ‘seven_seg’ in a separate file. This should allow for two digits (0 to F) to be displayed on the four seven-segment displays. This module should have the following ports:
  ▪ Two 4-bit inputs ‘a’ and ‘b’ and one 1-bit input ‘mux’
  ▪ A 7-bit output to drive the seven-segment cathodes and two 1-bit anodes to drive the two anodes
• Connect 4 slider switches to the ‘a’ and ‘b’ inputs of the seven_seg module.
• Connect the ‘mux’ input to a push-button switch.
• When the push-button is pressed, display the value of the lower 4-bits of the slider switches on seven-segment display #1
• When the push-button is released, display the value of the upper 4-bits of the slider switches on seven-segment display #2

Part 2:

• Create a new top_level module called ‘lab1_top’ in a second file that has inputs to the slider switches and push buttons, and outputs to the seven segment display.
  ▪ Instantiate the seven_seg module from part 1 into the top level module using named association
• Add additional Verilog statements to the top level module to add the following functionality (use two additional slider or push button switches for the four functions):
  • 00 – show the value of the 8-slider switches on the two seven-segment displays (like part 1)
• 01 – on seven-segment display #1 show the number ‘1’, on display #2 show the value of the logical operation of slider switches ‘a’ AND ‘b’
• 10 – on display #1 show the number ‘2’, on display #2 show the value of slider switches ‘a’ OR ‘b’
• 11 – on display #1 show the number ‘3’, on display #2 show the value of slider switches ‘a’ XOR ‘b’

(Use the same ‘mux’ push-button as before to display the first or second seven-segment displays)

Make sure the other two seven-segment displays are always off

Note: This is a combinational design, no clocks are required.

No lab report is required for this exercise but you need to hand in a hard (printed) copy of your two Verilog files (make sure you include a header with your name, date, and description – and add comments), and demo your working lab (part 2), and have your design signed-off during your lab session during the second week of class.

This lab is to be completed individually (future labs can be completed with a partner).

Reference Material

Complete the decoder tutorial.

Review the counter tutorial to see how to instantiate a lower-level module:

```verilog
// make a copy of the decoder component - named association
decoder d1 (.count(count), .seven seg(seven seg));
```

Read the Seven Segment section in the Basys3 Reference Manual.