TEST PREPARATION

This exam is closed book (no books or notes or electronic devices allowed).
Here are some Verilog keywords to remind you:

module, input, output, endmodule, assign, always, if, else, case, endcase, posedge, negedge

Do not use the wildcard character ‘*’ in the sensitivity list for an always statement – list all the appropriate signals.

Read each question carefully
Use a standard and consistent coding style.

Try and answer each question - if you consider any question to be ambiguous then state any assumptions you make.

NAME: ___________________________

ECE Box: ________________________

Question 1 [25 marks]: The function table of a 2-line to 4-line decoder with an enable input is:

<table>
<thead>
<tr>
<th>Enable</th>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>G</td>
<td>B</td>
</tr>
<tr>
<td>1</td>
<td>don’t care</td>
<td>don’t care</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Write a Verilog synthesizable module description of this decoder using:

A) An assign statement with the conditional operator.
B) An always statement with a CASE statement
Question 2 [20 marks]: Write the Verilog synthesizable module description of a 6-bit priority encoder. The six inputs are i0 to i5 with i5 having the highest priority input. There are two outputs, ‘a’, and ‘gs’. The output ‘a’ should encode the address of the highest priority input (‘000’ to ‘101’) and the ‘gs’ output should be ‘1’ when at least one of the inputs is ‘1’.

Question 3 [20 marks]: Write the Verilog synthesizable module description of a counter with an asynchronous reset (active high) signal. The counter should count from 8 to 88 on a negative edge of a clock but only when an enable signal (called ‘clk_enable’) is high. Once the counter gets to 88 it should restart at 8.

Question 4 [35 marks]: It is important to use a common clock in FPGA logic designs so that the high-speed low-skew dedicated clock routing resources can be used. Keeping this principle in mind, design the following:

Assume that an FPGA has a 50MHz master clock (clk_50M). Write an always statement to generate a 12-bit LFSR that shifts at the 1MHz rate (derived from the 50MHz clock). The LFSR should be loaded with all ‘1’s on reset (active high, asynchronous reset). The output is taken from the least significant stage (bit 0). It has two feedback taps from bits 4 and 8 that feedback an exclusive-or to the most significant stage (bit 11). The LFSR shifts on a positive edge of the clock signal.

The start of the module description is provided:

```verilog
module lfsr (
    input  clk_50M,
    input  reset
    output q
);
```