

(Rev. 0.2/9/19/05)

Xilinx ISE and Spartan-3 Tutorial

for Xilinx ISE 7.1i the Digilent / Xilinx Spartan-3 Starter Board

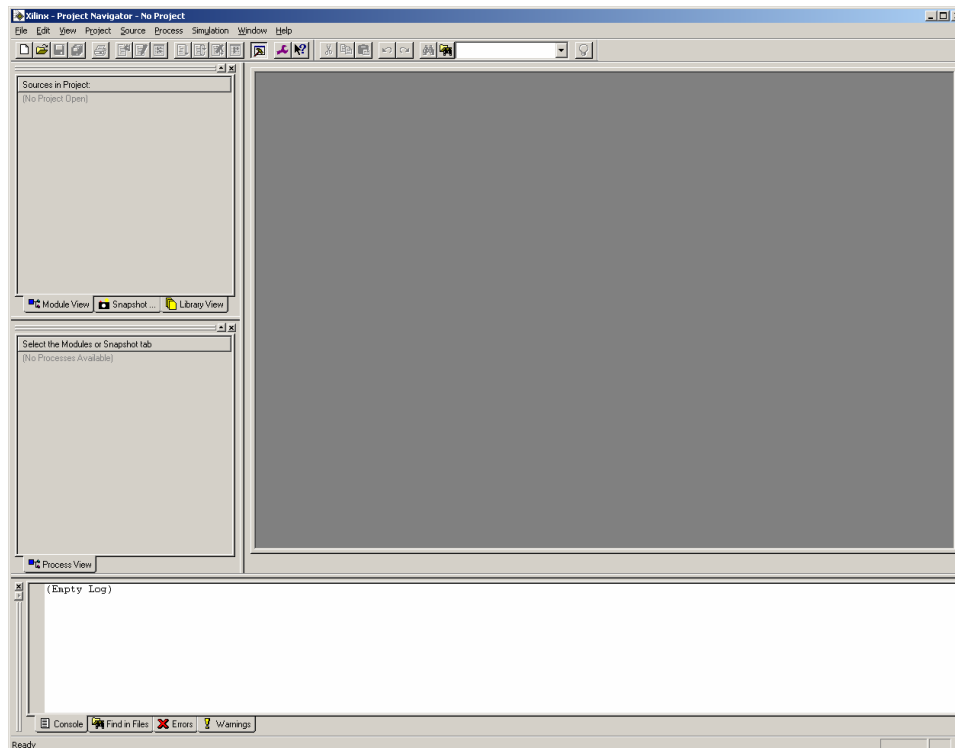
Introduction

This tutorial will show you how to create a simple Xilinx ISE project based on the Spartan-3 Board. We will be implementing a simple decoder circuit that uses the switches on the board as inputs and the eight LEDs as outputs. There are several parts to this tutorial. Part 1 shows the basics of creating a project in Xilinx ISE. Part 2 shows how to create a PROM file that can be written to the non-volatile memory on the Spartan-3 board (because the FPGA's configuration is lost when power is turned off). Part 3 shows how to then program the board.

Part 1: Starting a new Project

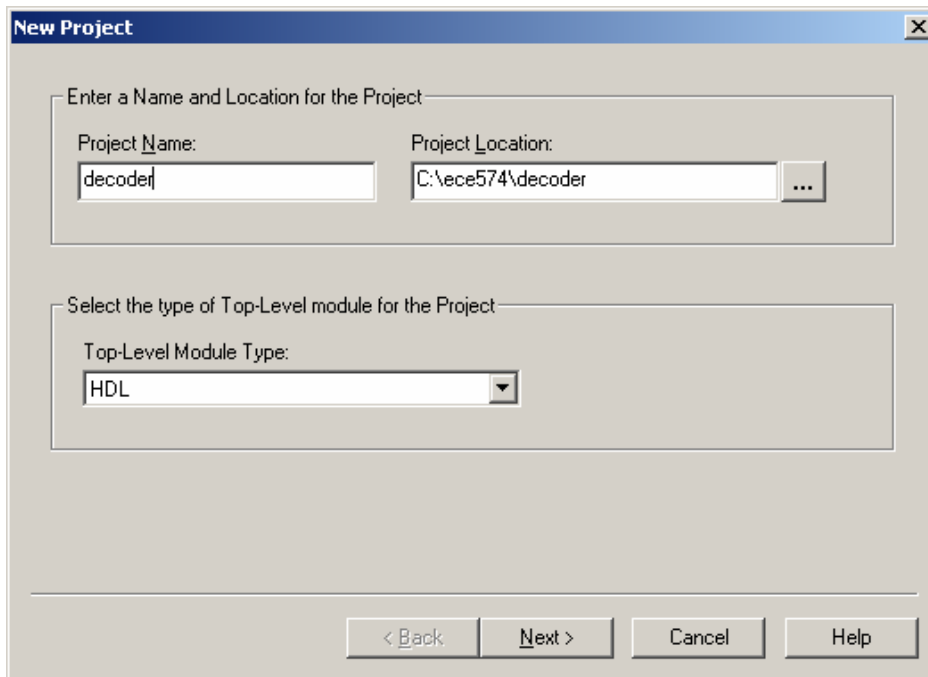


Start the **Xilinx ISE 7.1i** Project Navigator:



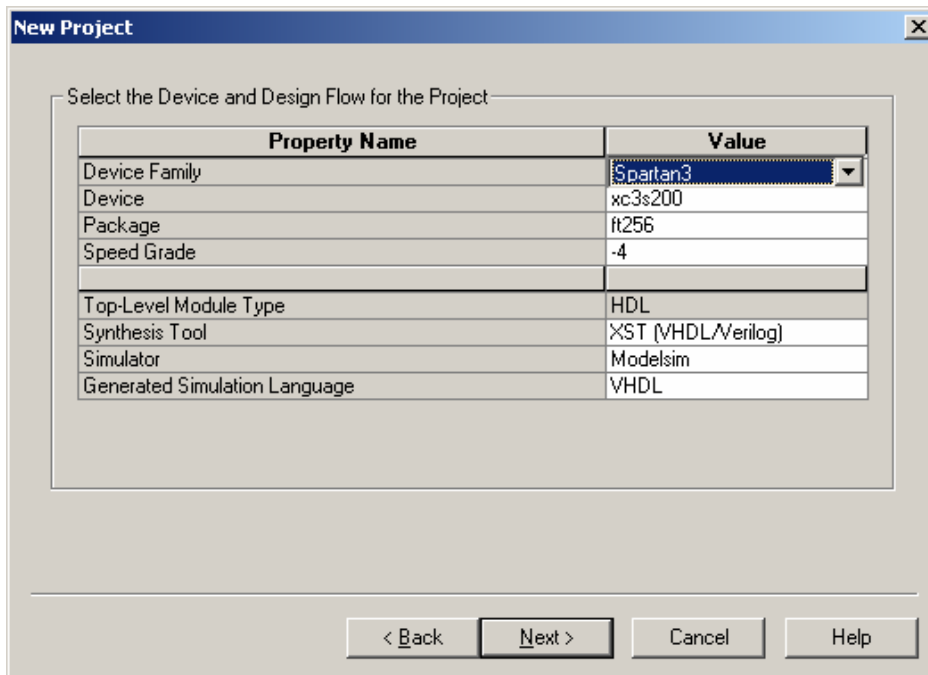
Select **File** → **New Project**.

Select a project location and name. For this tutorial we will name the project “**decoder**”:

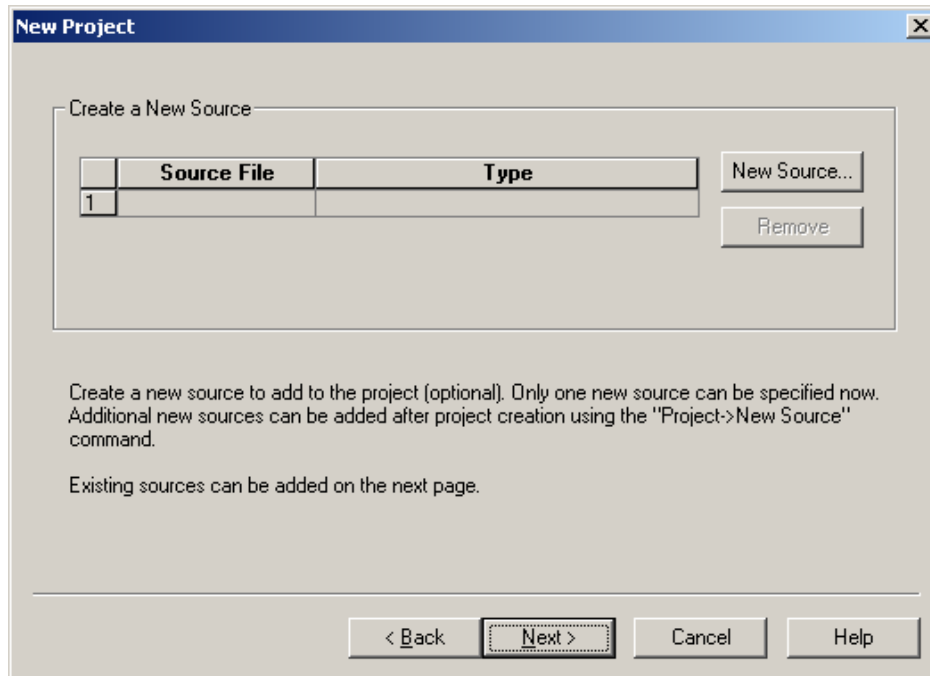


Click **Next**.

Select the device family, device, package, and speed grade, as shown here:

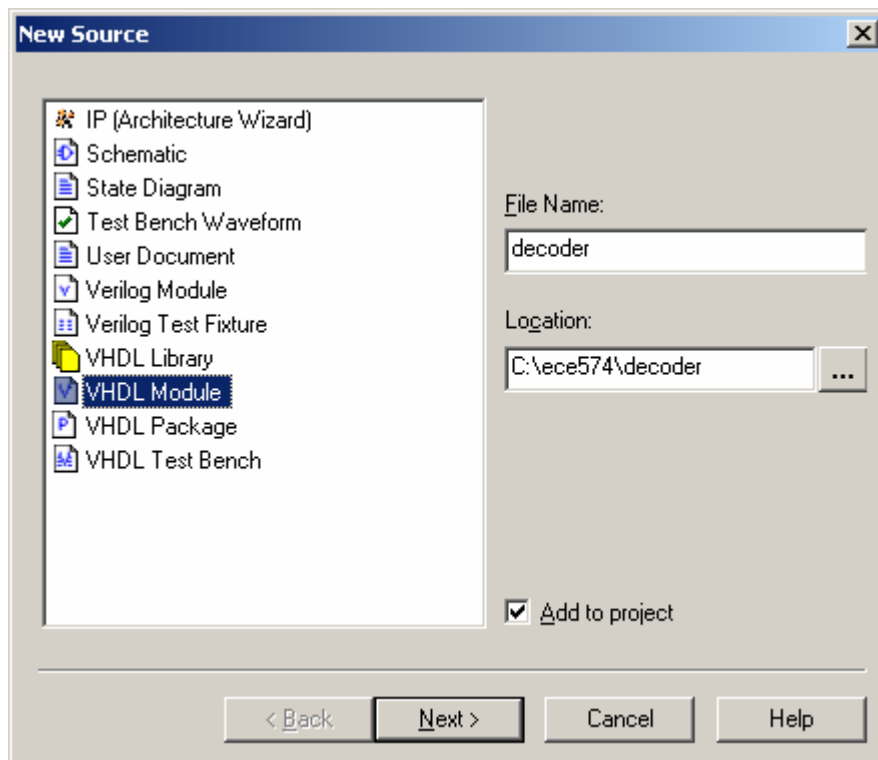


Click **Next**.



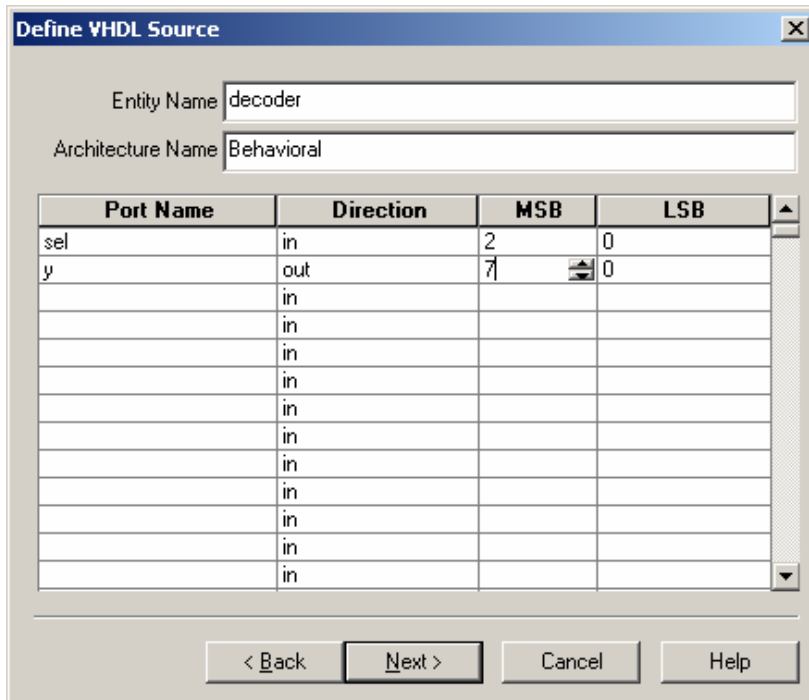
Click **New Source**.

Select VHDL Module and enter “**decoder**” as the file name:

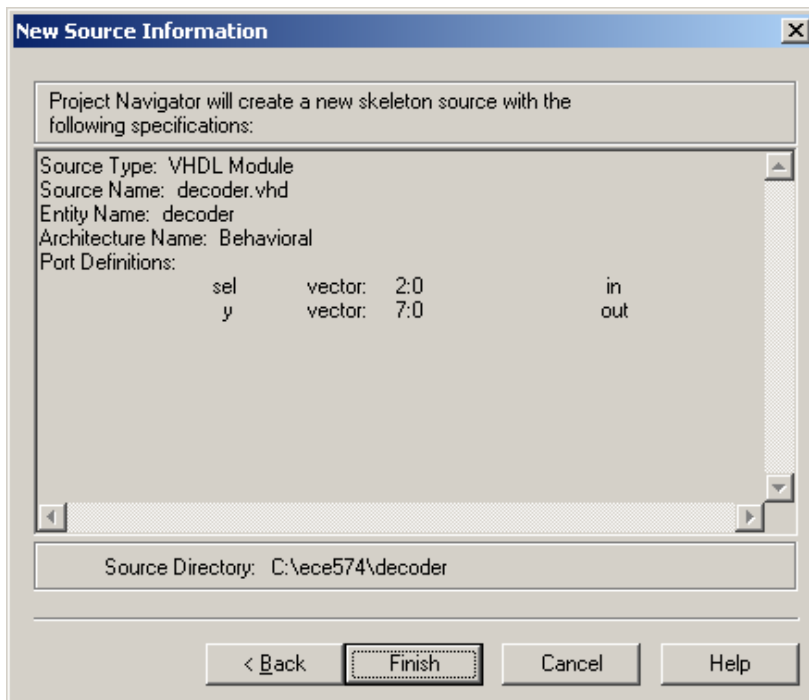


Click **Next**.

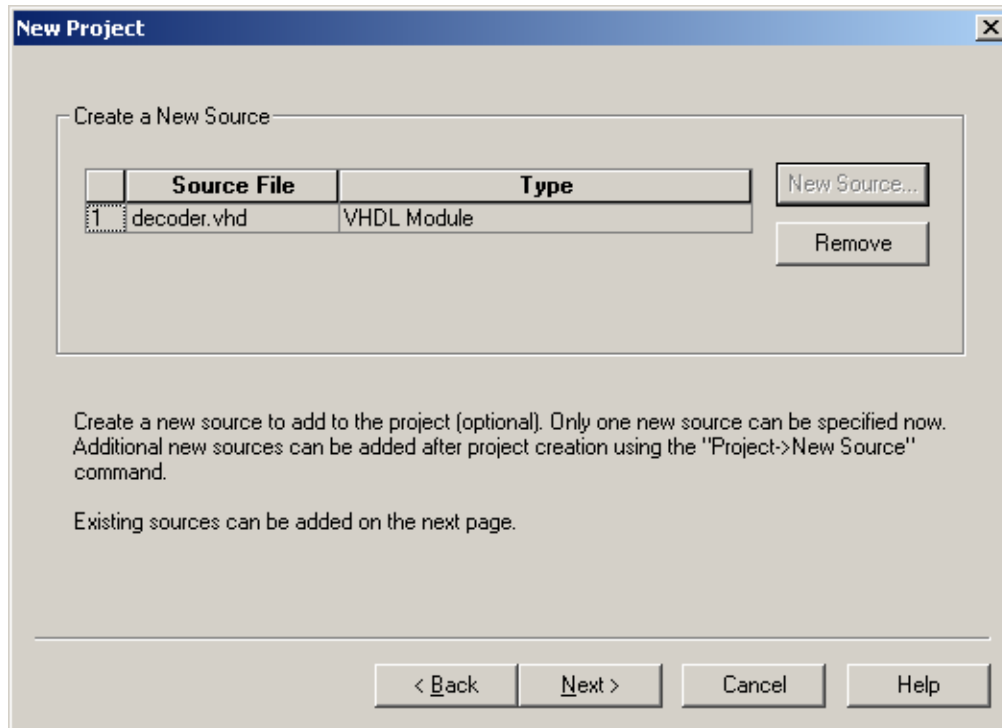
You can now specify the inputs and outputs for the decoder. These will be inserted into an automatically generated template for the VHDL file. We have one 3-bit input (“sel”) and one 8-bit output (“y”):



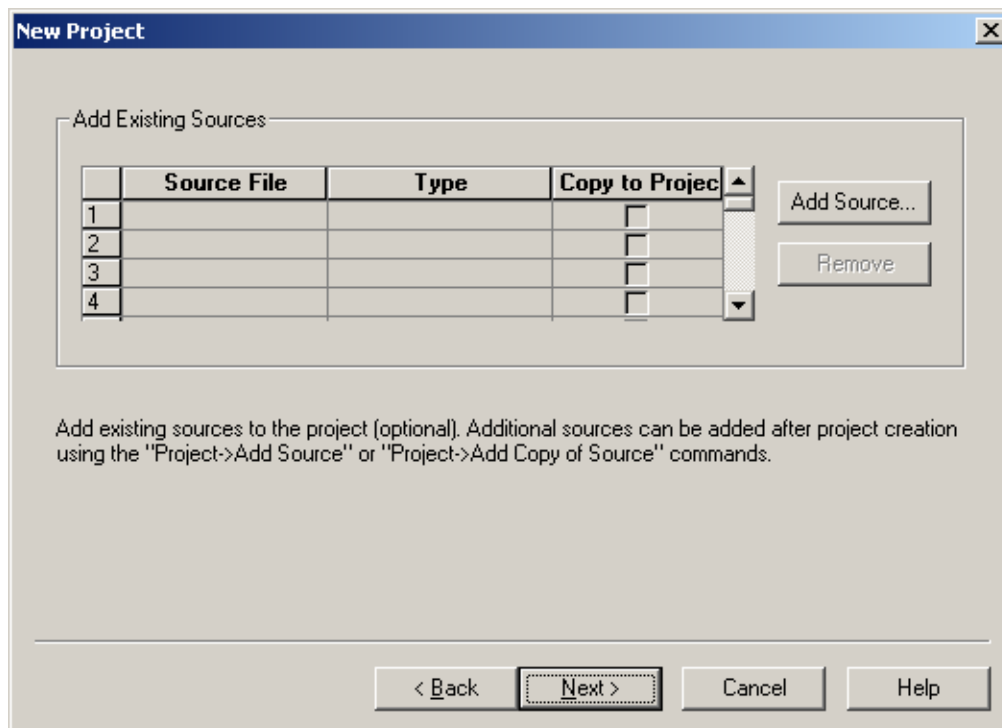
Click **Next**. You will be shown a summary window:



Click **Finish**.

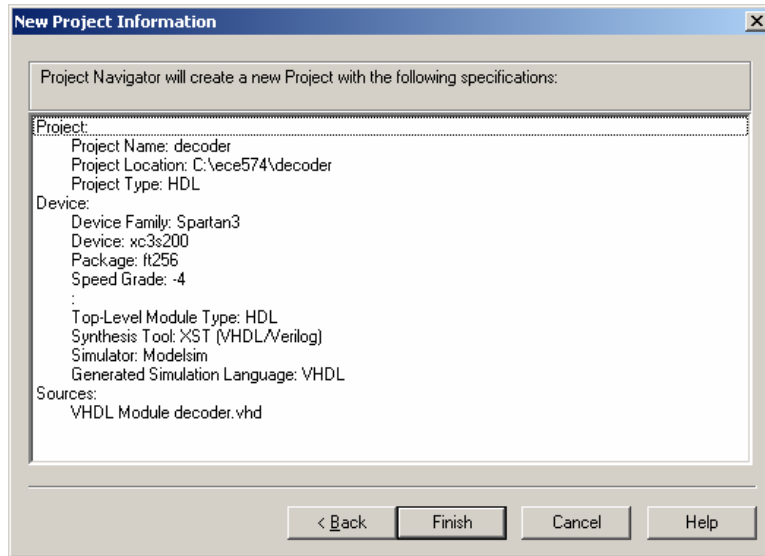


Click **Next**.



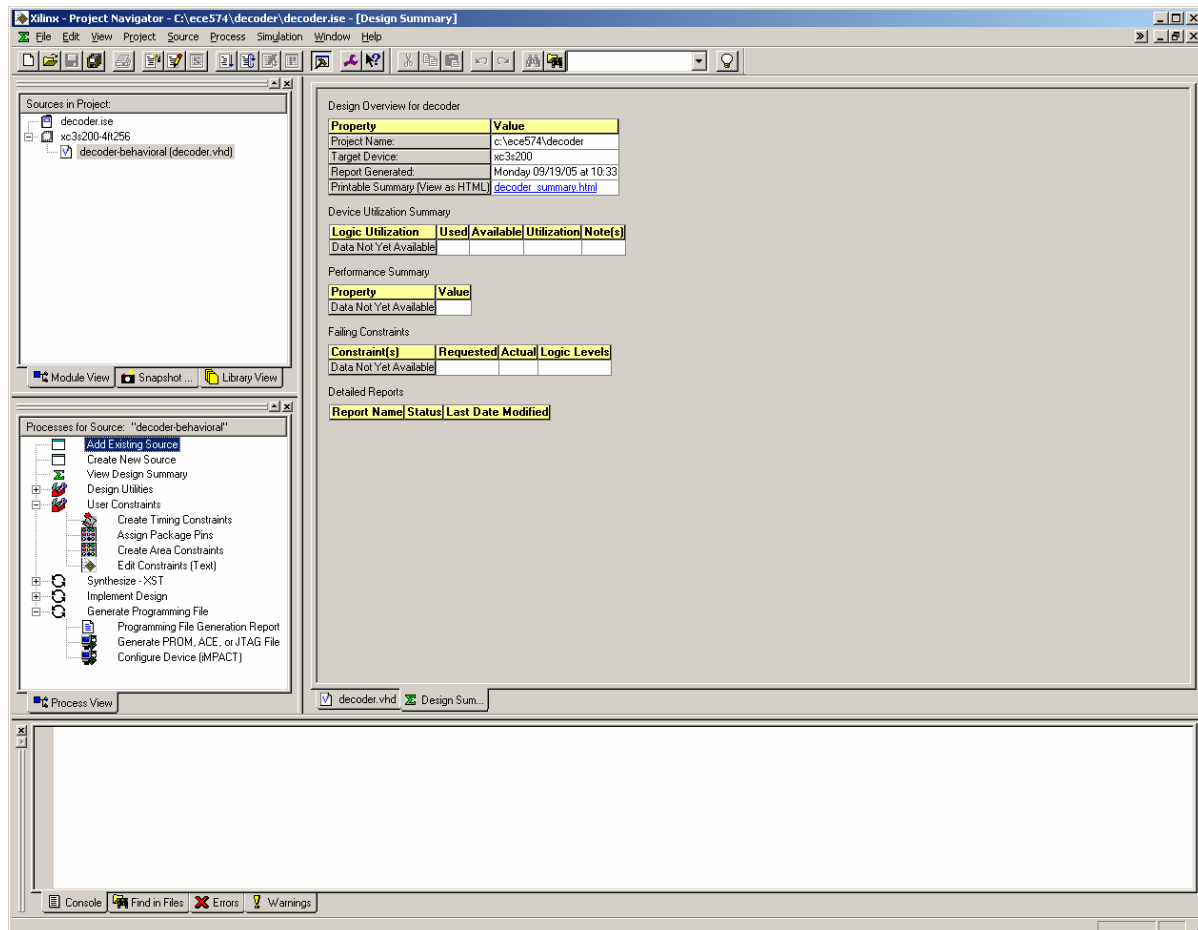
We do not have any existing sources, so click **Next**.

A summary window is shown:



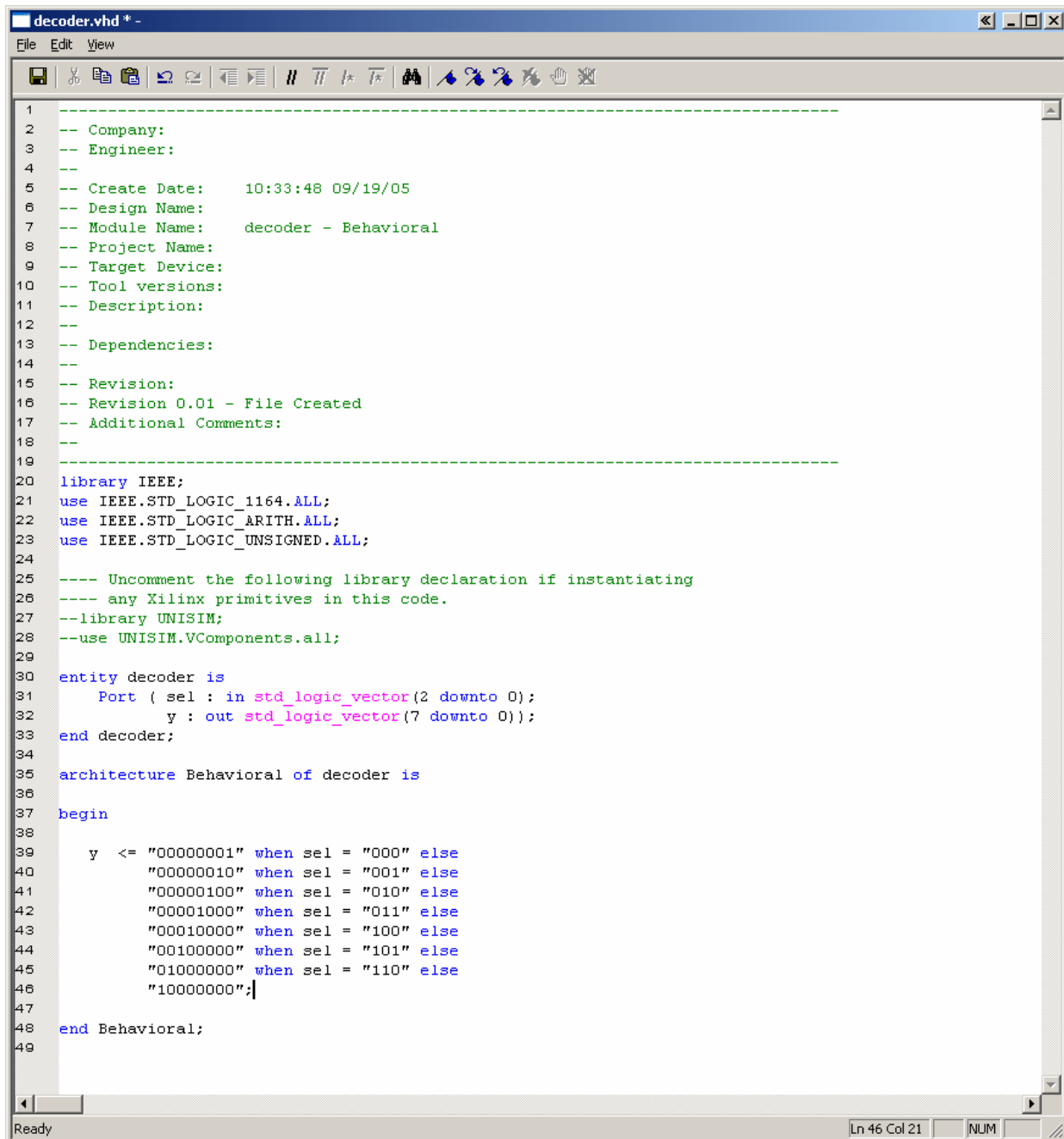
Click **Finish**.

Project Navigator now shows you a summary of the project:



Click on the “**decoder.vhd**” tab below the summary window, or double-click on “decoder-behavioral” in the top left “Sources” pane.

You will need to describe the behavior of the decoder using statements in the architecture body. In this example we will use a *conditional signal assignment statement*:

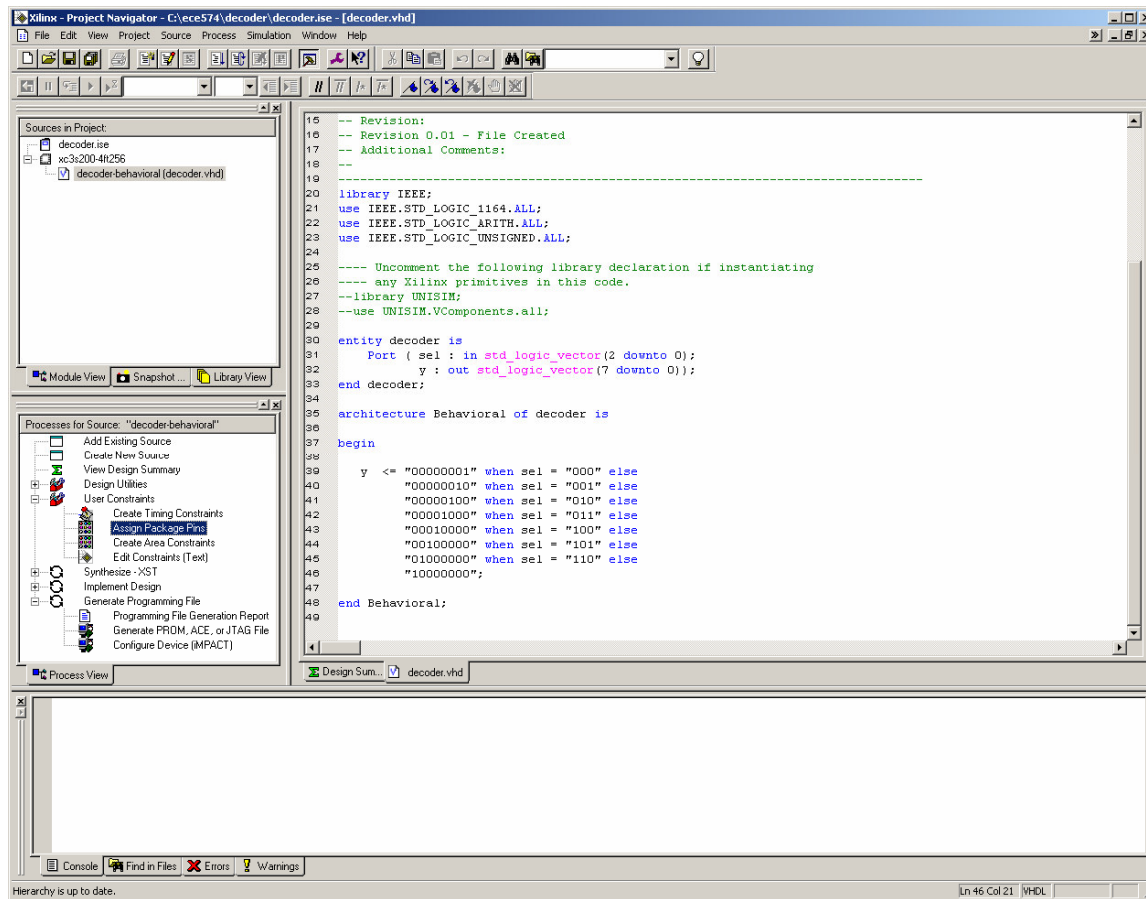


```

1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    10:33:48 09/19/05
6  -- Design Name:
7  -- Module Name:    decoder - Behavioral
8  -- Project Name:
9  -- Target Device:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25 ---- Uncomment the following library declaration if instantiating
26 ---- any Xilinx primitives in this code.
27 --library UNISIM;
28 --use UNISIM.VComponents.all;
29
30 entity decoder is
31     Port ( sel : in std_logic_vector(2 downto 0);
32           y : out std_logic_vector(7 downto 0));
33 end decoder;
34
35 architecture Behavioral of decoder is
36
37 begin
38
39     y <= "00000001" when sel = "000" else
40         "00000010" when sel = "001" else
41         "00000100" when sel = "010" else
42         "00001000" when sel = "011" else
43         "00010000" when sel = "100" else
44         "00100000" when sel = "101" else
45         "01000000" when sel = "110" else
46         "10000000";
47
48 end Behavioral;
49

```

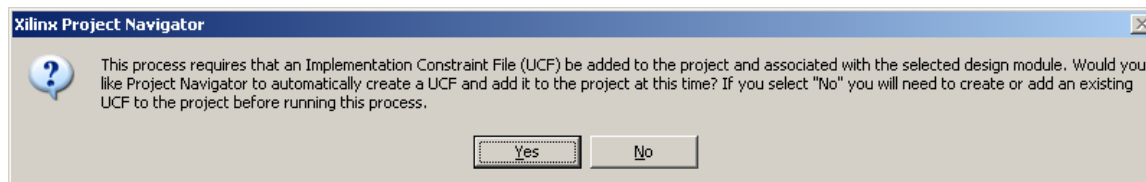
Before we can synthesize this design we need to specify what pins on the FPGA the inputs and outputs are connected to.



Double-Click on “Assign Package Pins” in the “Processes” pane in the left of the window.

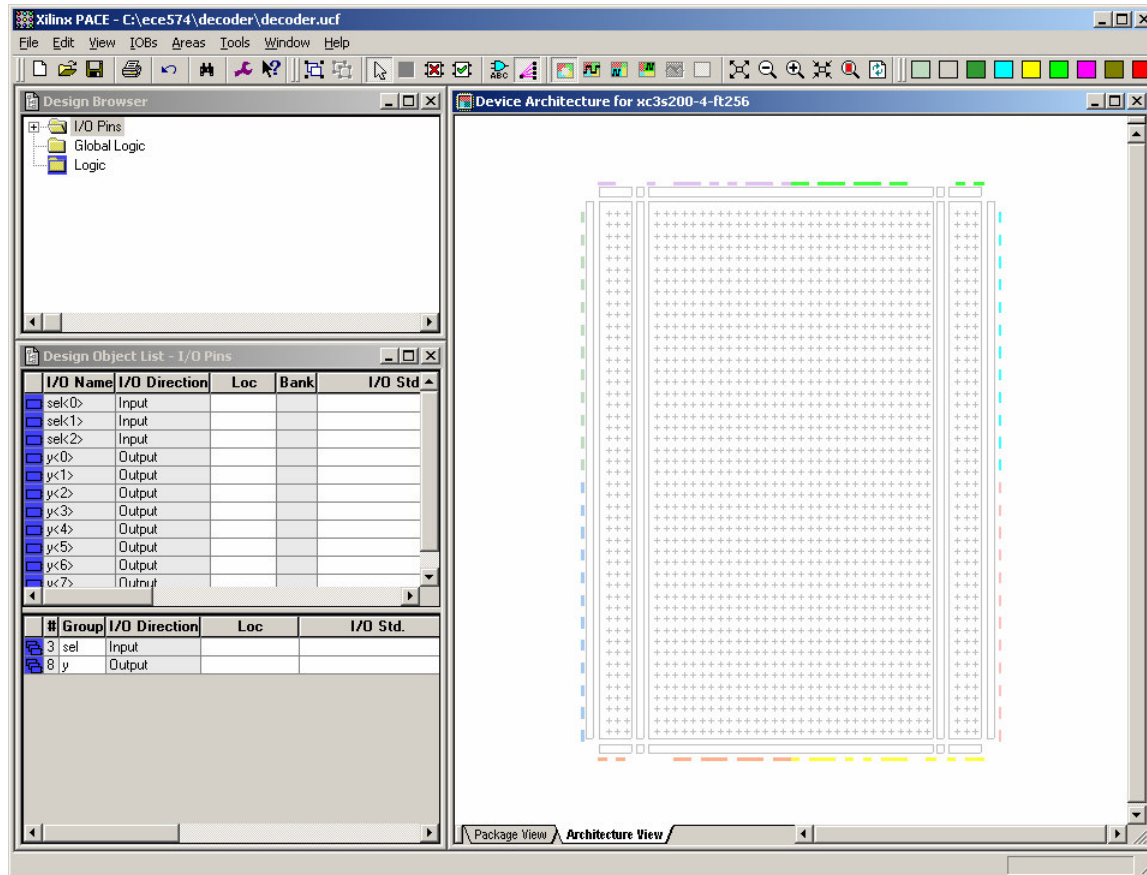
Note: You may be asked to save the VHDL file, and your design will be checked for syntax errors (these will need to be fixed before you can proceed).

The tools will prompt you to create a UCF file:

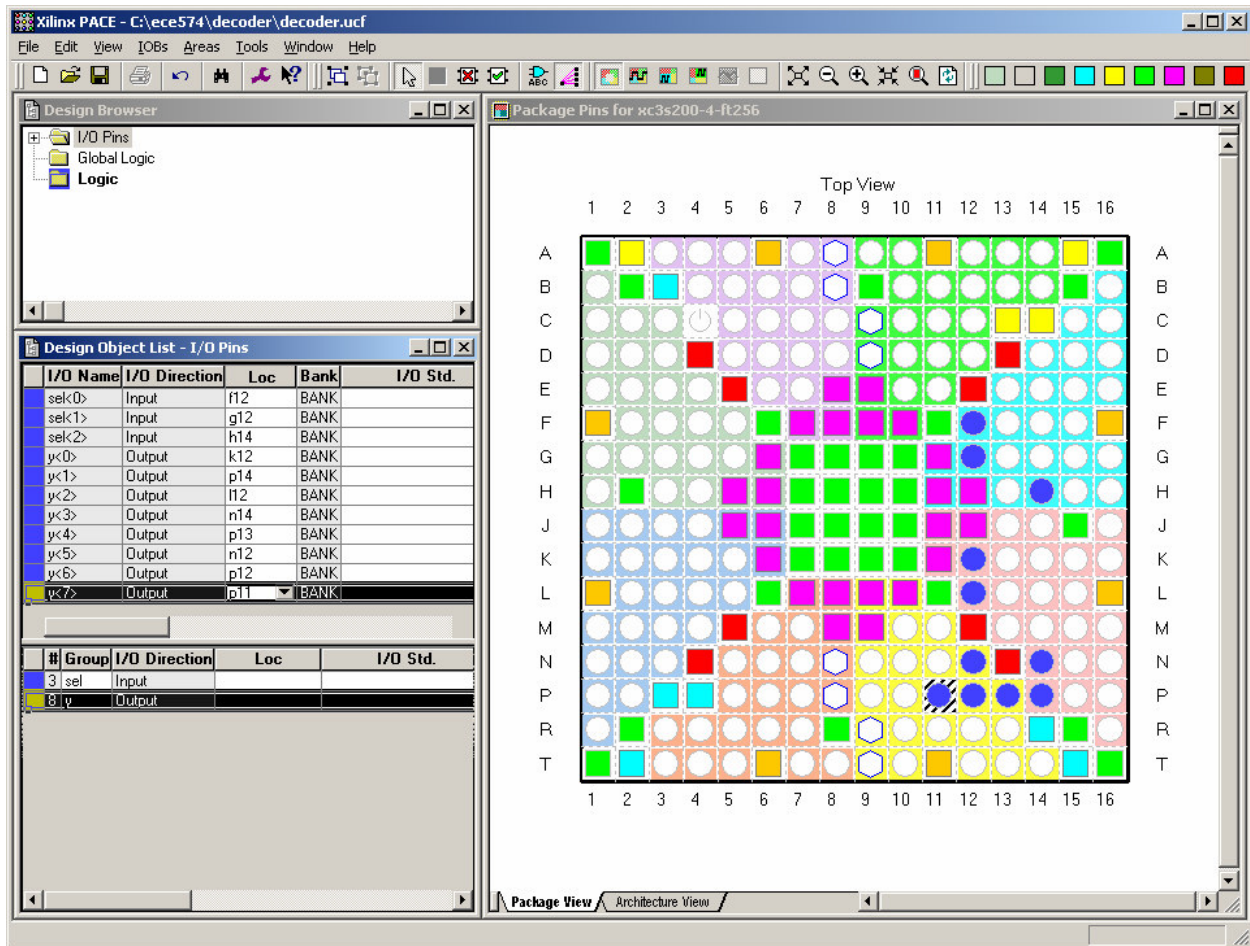


Click **Yes**.

The PACE editor will load:

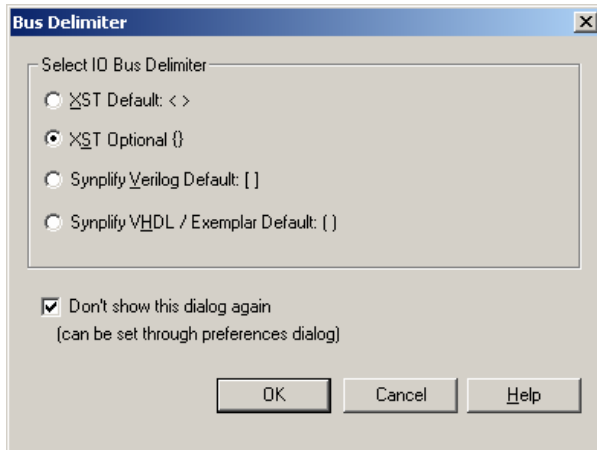


Select “**Package View**” at the bottom of the right pane (this simply gives a better view of the physical FPGA package), and enter the pin names for each signal in the “**Design Object List**” at the left as shown here:



Click **File** → **Save** followed by **File** → **Exit**.

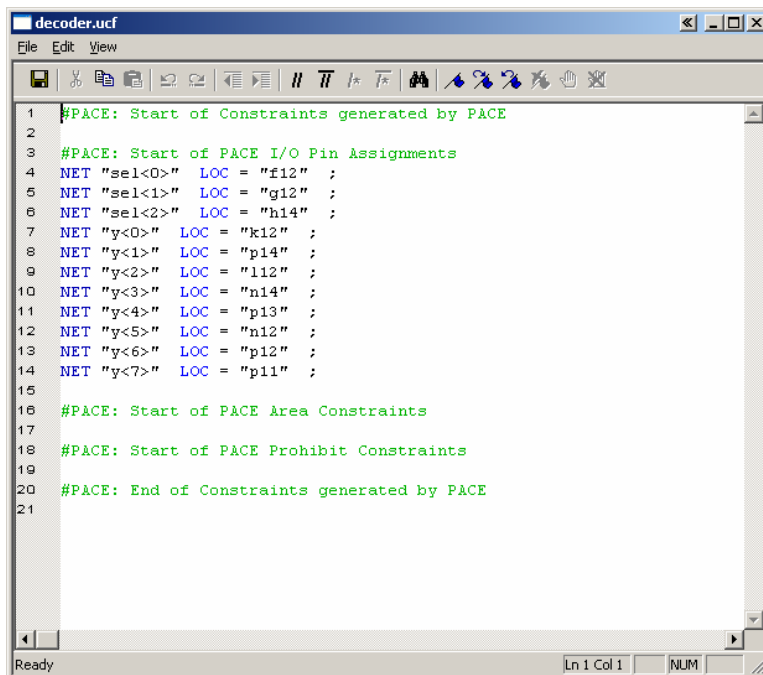
Note: The following dialog may appear when saving the file:



Select “Don’t show this dialog again” and click **Ok**.

Note: You may notice that the items listed in the “Processes” pane have changed. The “Processes” pane shows the actions that can be run on the file that is currently selected in the “Sources” pane. Select the “decoder-behavioral” source to get the same actions that were previously shown.

You can then view the UCF file by double-clicking “Edit Constraints (Text)” in the Project Navigator:



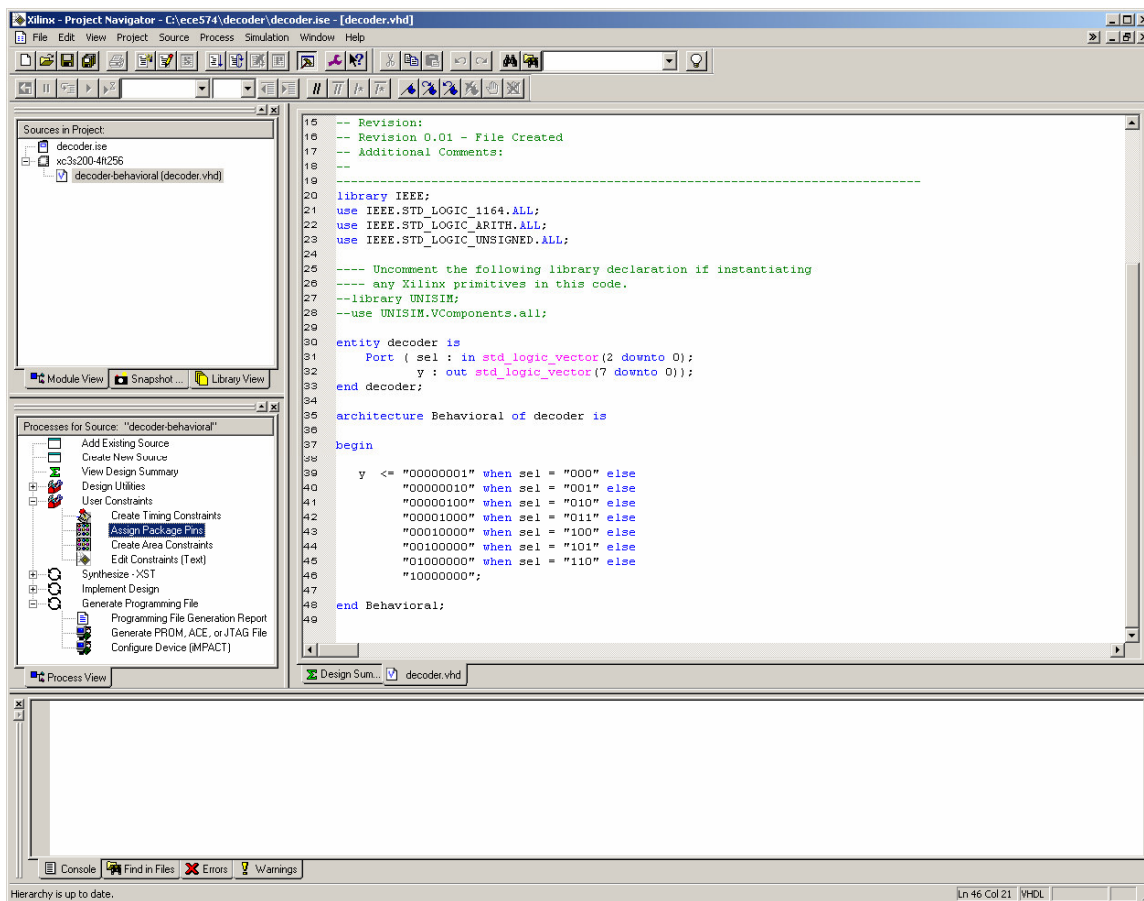
You are now ready to generate a PROM file and/or program the FPGA.

Part 2: Generating a PROM File

In this part of the tutorial, we will see how to generate a PROM file that can be written to the Platform Flash on the Spartan-3 board, so that your FPGA's configuration is saved even when the board is powered down.

If you do not want to generate a PROM file, you can skip directly to Part 3. However, in the interest of this tutorial we recommend you complete this part as well.

We assume you are continuing from Part 1 above and are still in Project Navigator:



Double-click on “**Generate PROM, ACE, or JTAG File**” in the “Processes” pane. You will notice that Project Navigator will execute the steps listed above “Generate Programming File” (Synthesis and Implement Design) and mark them with a green checkmark as they complete.

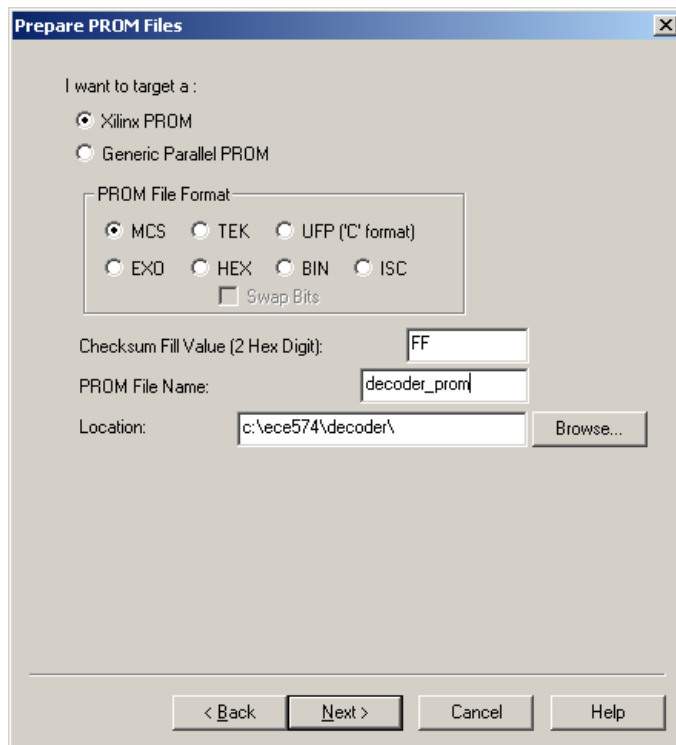
The iMPACT tool will open and a wizard to create a new configuration will open.

Select **PROM File**:



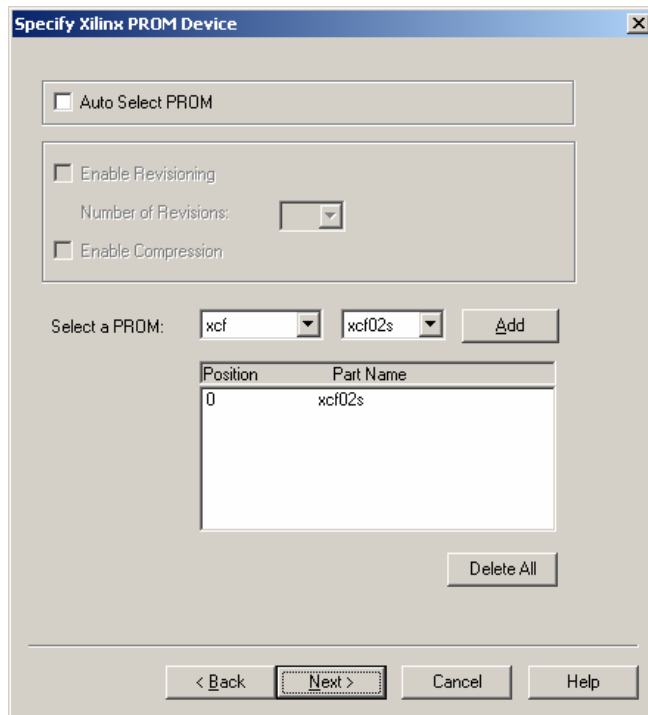
Click **Next**.

Enter the **PROM File Name** (for example, "decoder_prom"):



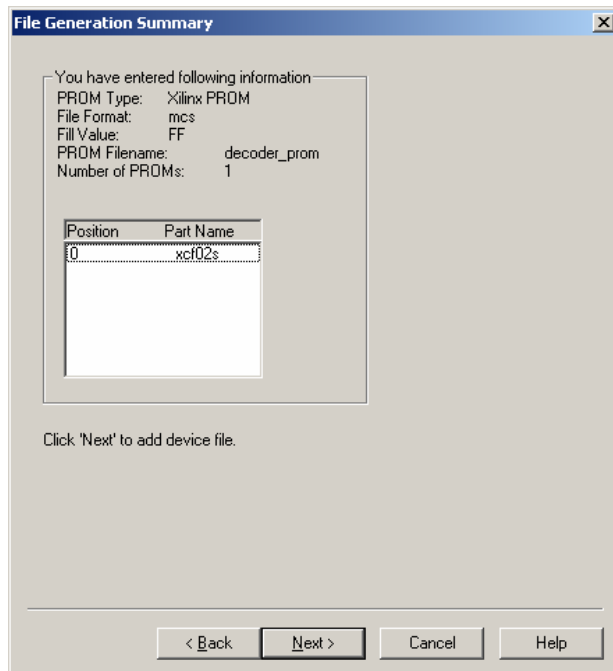
Click **Next**.

Select the appropriate PROM (which is “xcf” / “**xcf02s**” for this board) from the dropdown menus and click **Add**:

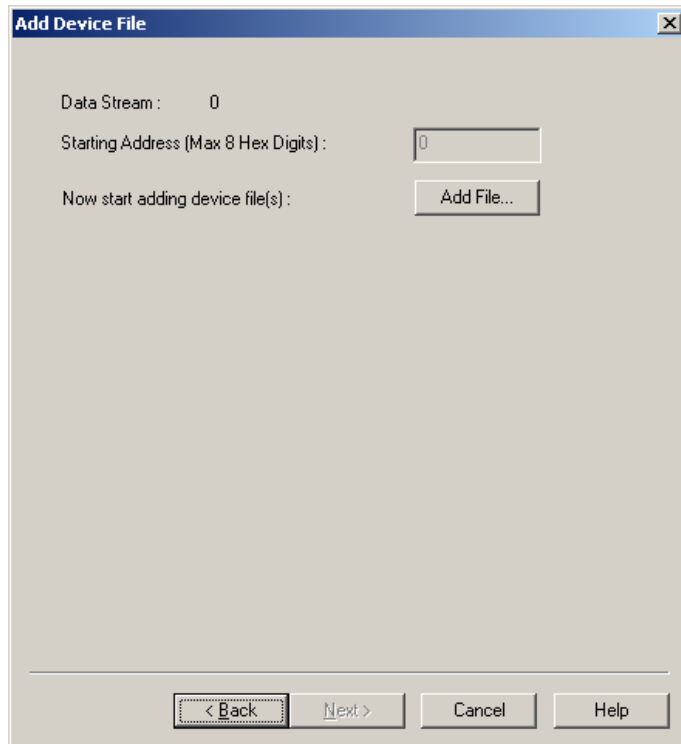


Click **Next**.

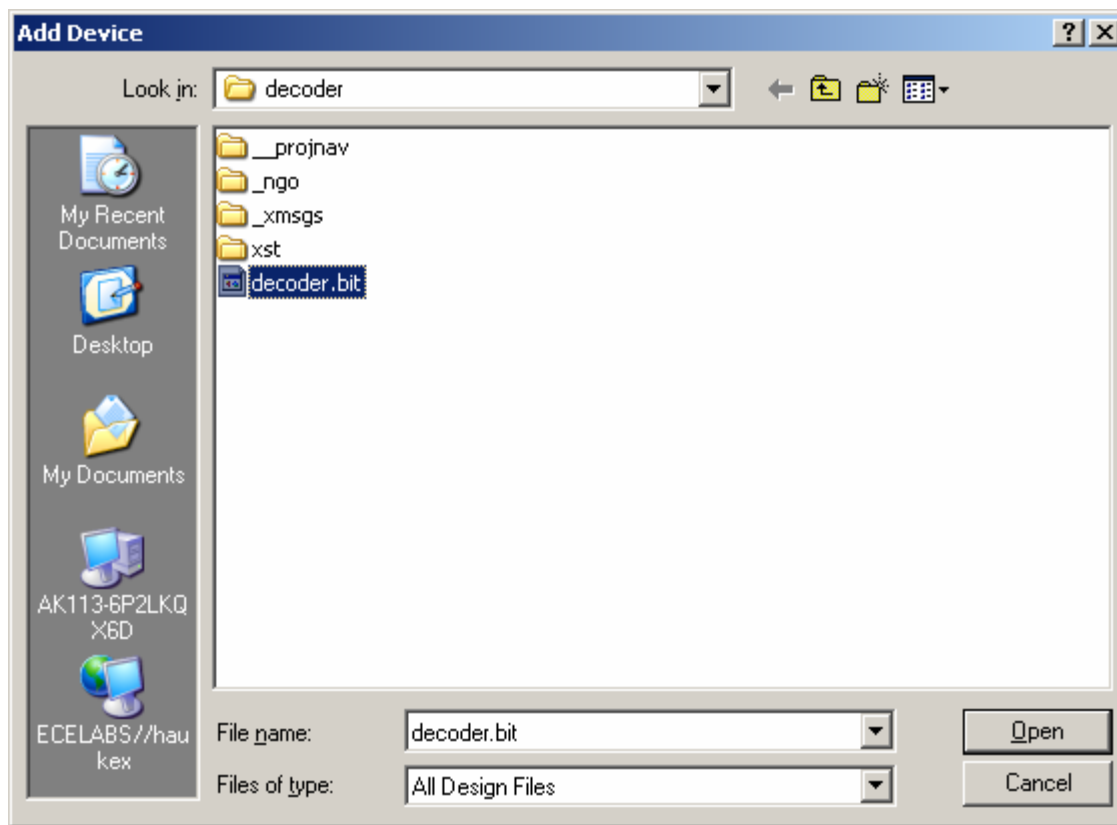
You will be shown a summary:



Click **Next**.

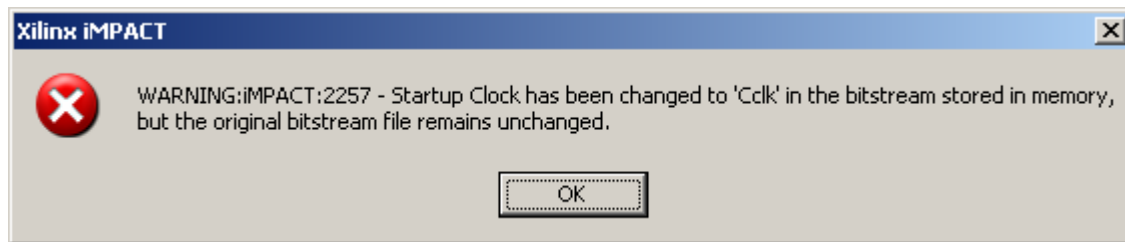


Click **Add File**.

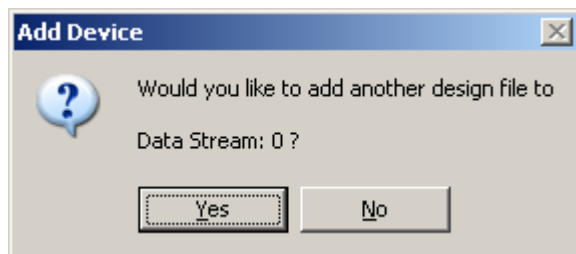


Select the “**decoder.bit**” file and click **Open**.

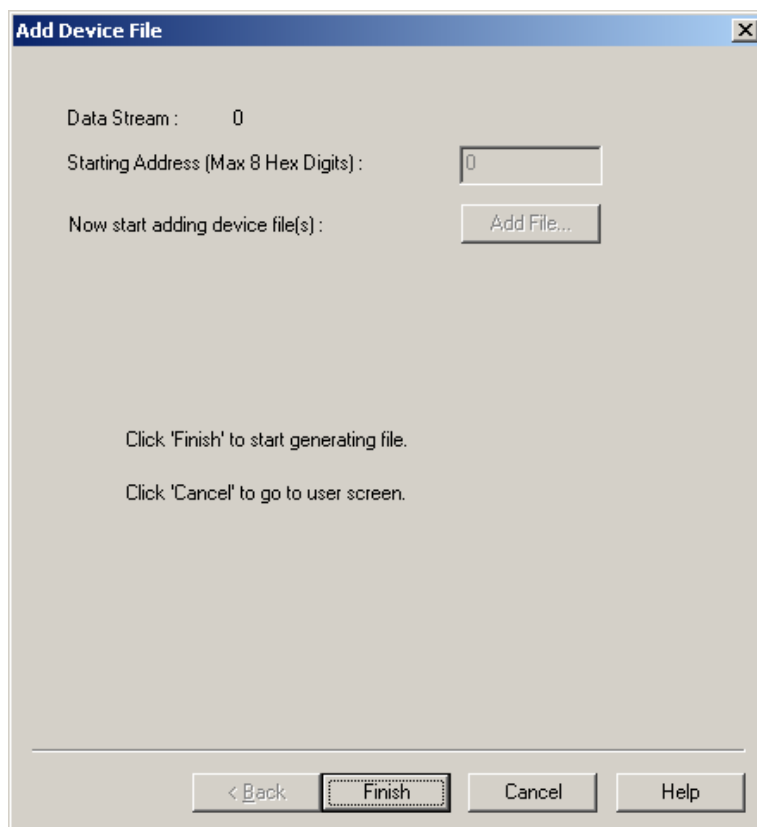
You *may* get the following warning message:



Simply click **Ok**.

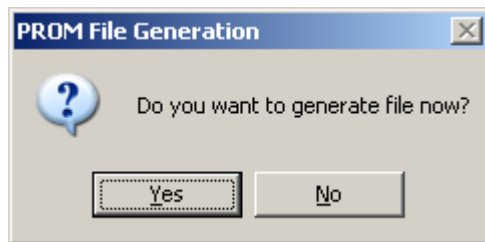


Click **No**.



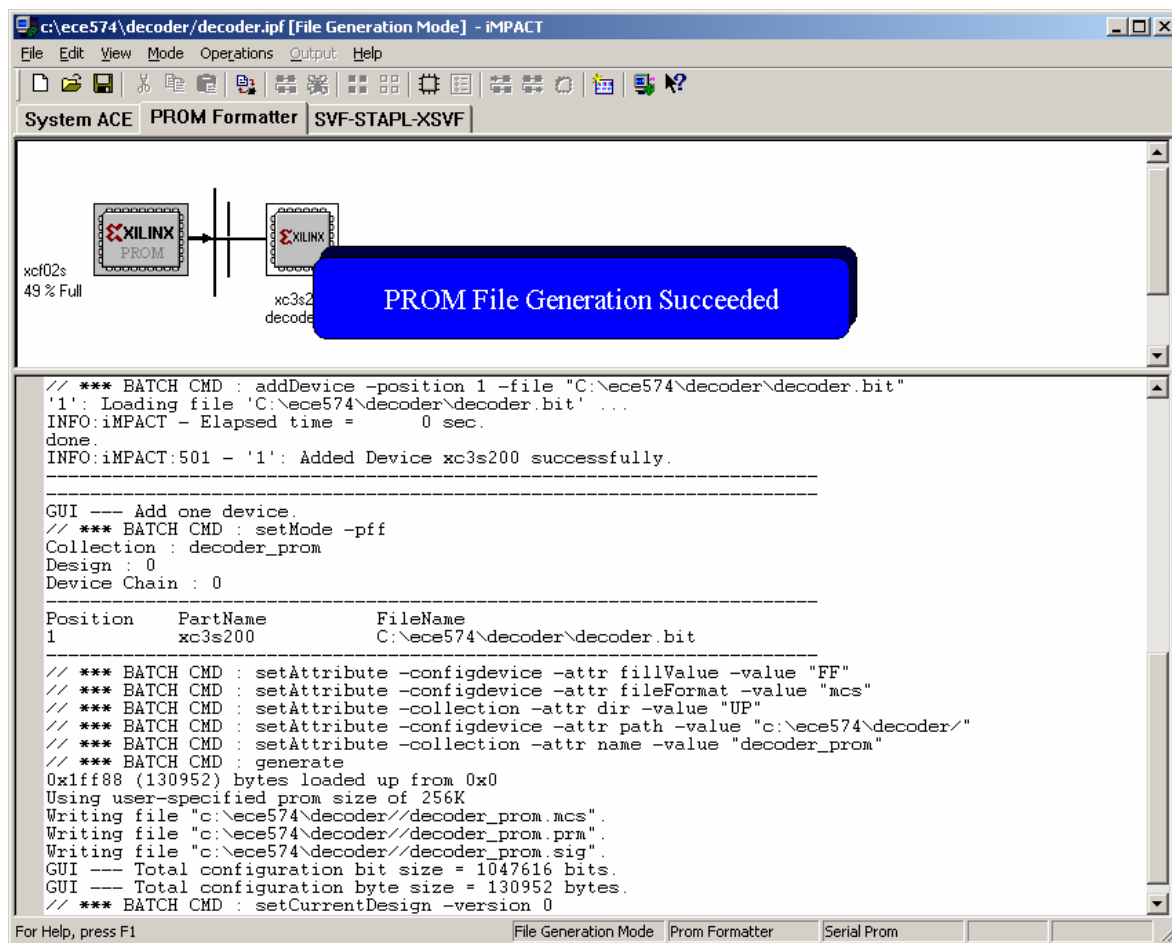
You can now click **Finish**.

iMPACT will ask:

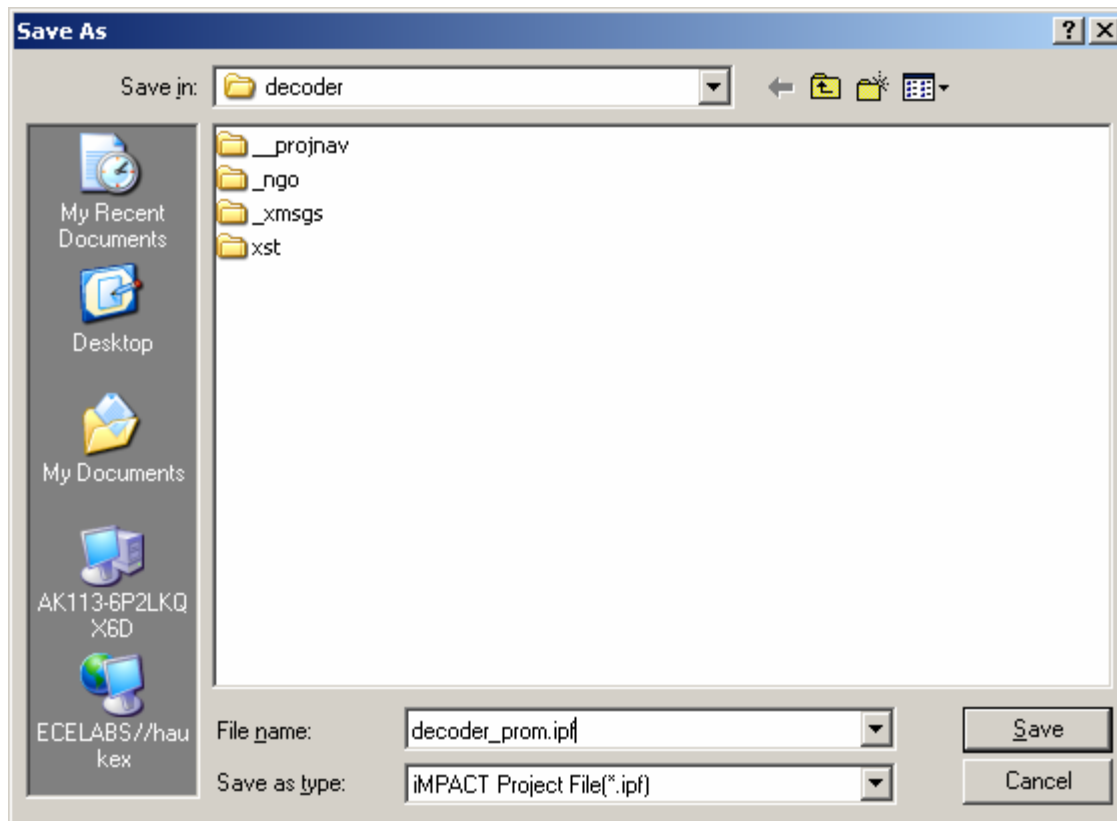


Select **Yes**.

You should then see iMPACT report successful file generation:



Before you close iMPACT, select **File** → **Save Project As...**



Save the configuration under a filename such as “decoder_prom.ipf”, but do *not* use the default filename of “decoder.ipf” (if you follow Part 2a below, remember this filename).

You can now close iMPACT.

Part 2a: Automatic PROM File Generation

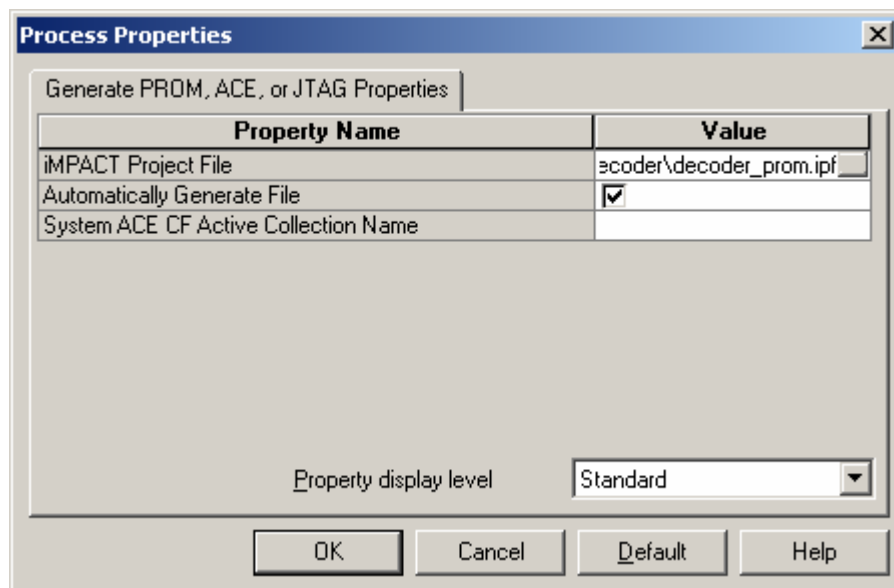
Now that the configuration is saved, we can have Project Navigator automatically create the PROM file without having to open iMPACT.

Warning: The settings we make in this part of the tutorial are global to the project. This means that in larger projects where you have multiple bit streams, making these settings will likely cause some confusion in generating the PROM file. In such projects you should not follow this part of the tutorial and rather follow the steps in Part 2 every time you generate the PROM file.

However, for this class all your projects should be simple enough for you to be able to use this method of automatic PROM file generation.

In the Project Navigator, *right-click* on “**Generate PROM, ACE, or JTAG File**” in the “Processes” pane and select “**Properties**”.

In the Process Properties window that opens, set the “**iMPACT Project File**” to the “decoder_prom.ipf” file that you saved at the end of Part 2. This will cause iMPACT to always load this configuration. To enable automatic file generation (iMPACT will not open, but the PROM file simply created in batch mode), turn on “**Automatically Generate File**”.



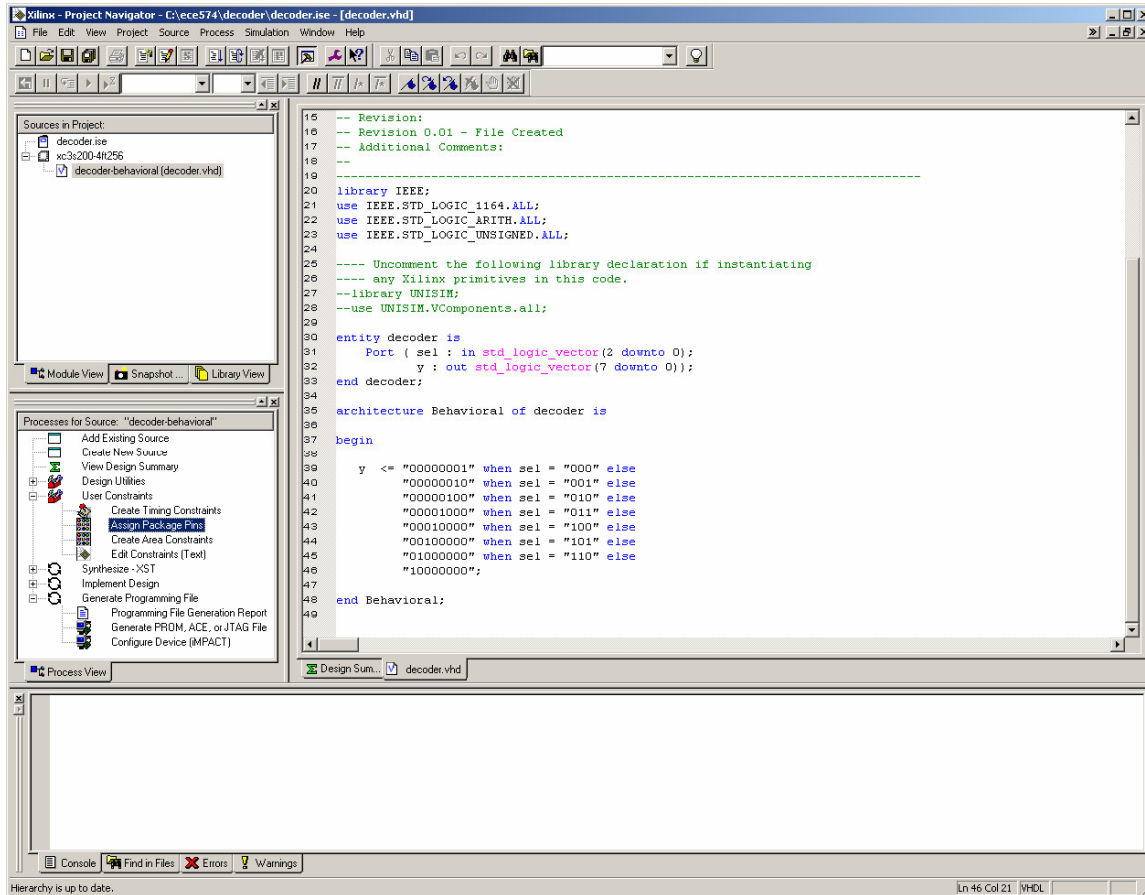
Click **Ok** to apply these settings.

Now, anytime you double-click “Generate PROM, ACE or JTAG File”, the PROM file will be automatically created.

Part 3: Programming the Board

In this part of the tutorial, we will show you how to actually program your design to the FPGA. Make sure that your JTAG cable is plugged into your PC and the board, and that the board is powered up.

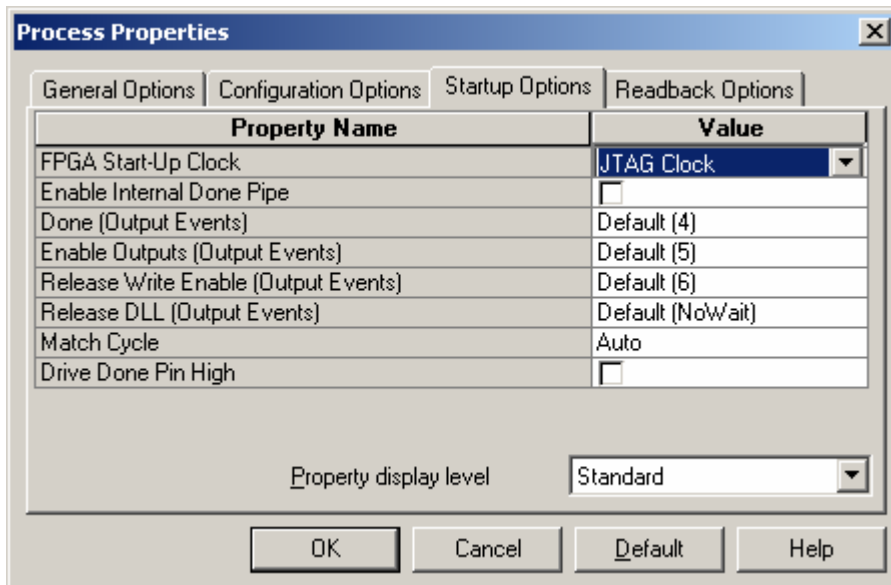
We assume you are continuing from Part 1 or Part 2 above and are still in Project Navigator:



Note that this following step of changing the Start-Up Clock is not absolutely necessary because iMPACT will automatically pick the correct clock, but doing the following avoids a warning message telling you about this every time you program the board.

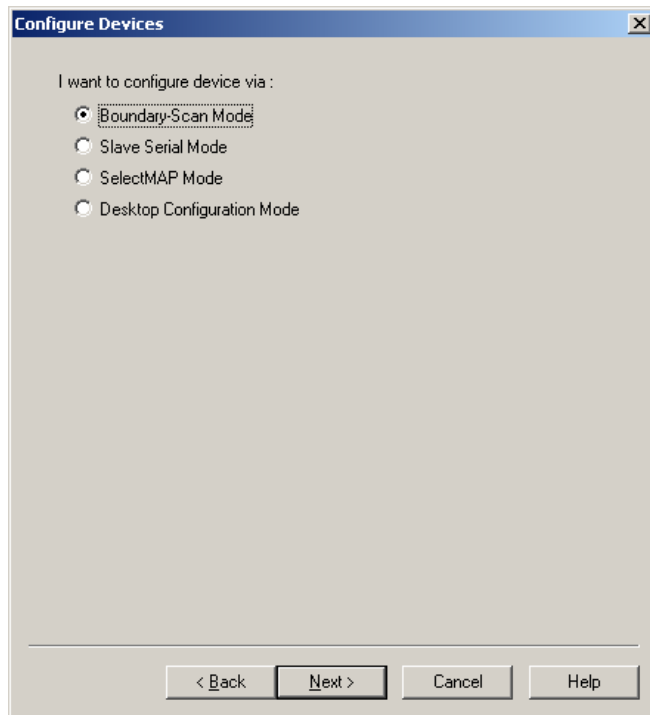
Right-click on “**Generate Programming File**” in the “Processes” pane and select “**Properties**”. In the “Process Properties” window that opens, select the “**Startup Options**” tab.

Change the “**FPGA Start-Up Clock**” to “**JTAG Clock**”.

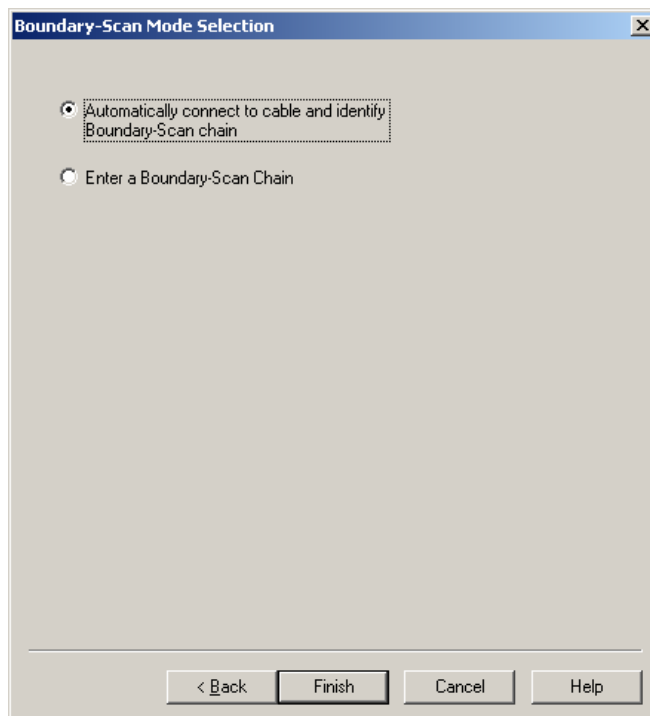


Click **Ok**.

Double-click on “**Configure Device (iMPACT)**”. The iMPACT tool will open and a wizard to create a new configuration will open.

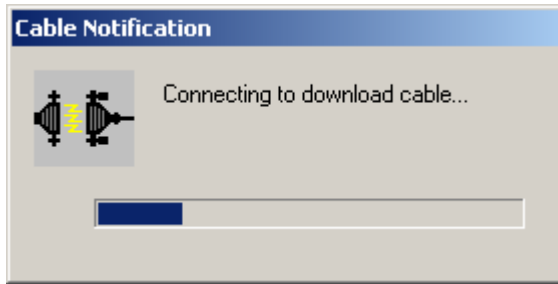


Click **Next**.

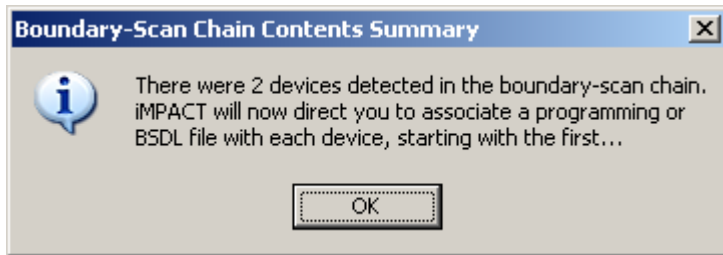


Click **Next**.

The following window will briefly show:



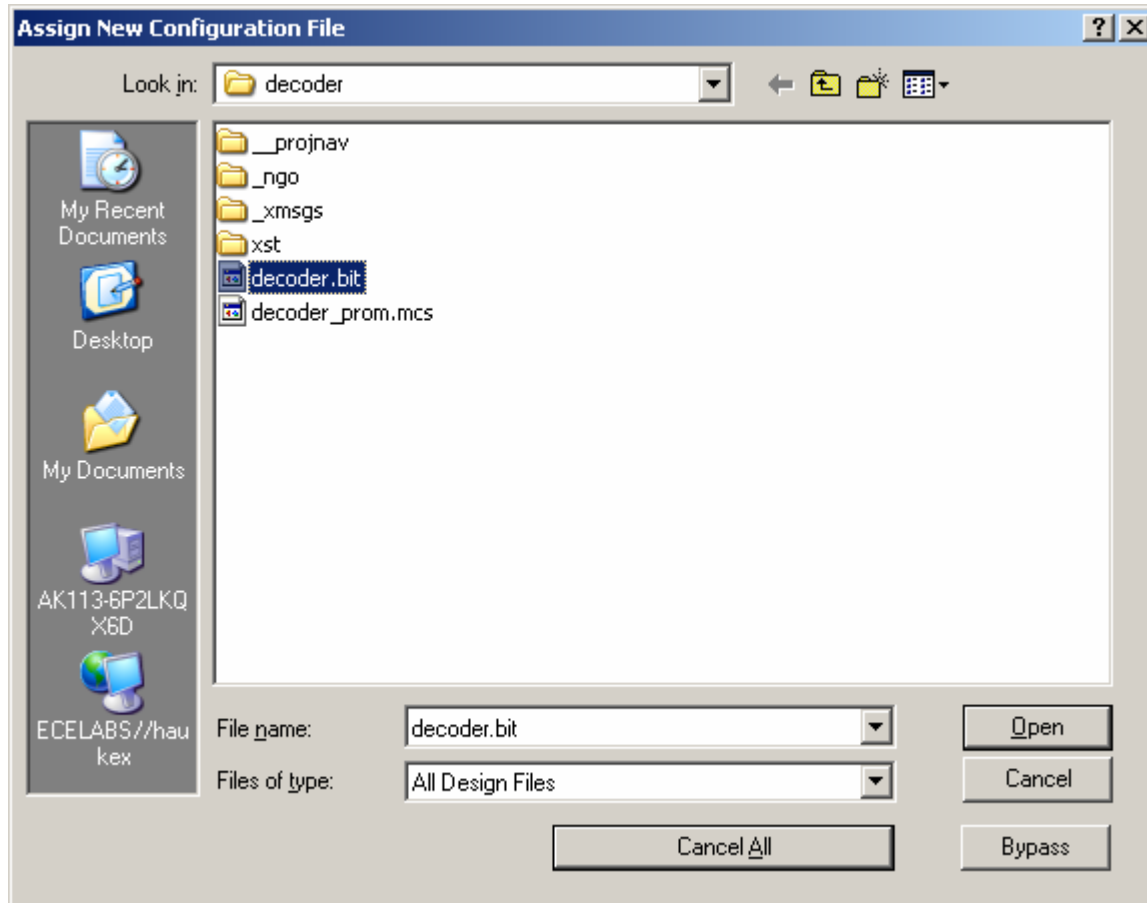
iMPACT will inform you that it has found the devices on the board:



You can now select the configuration files that will be programmed to the parts.

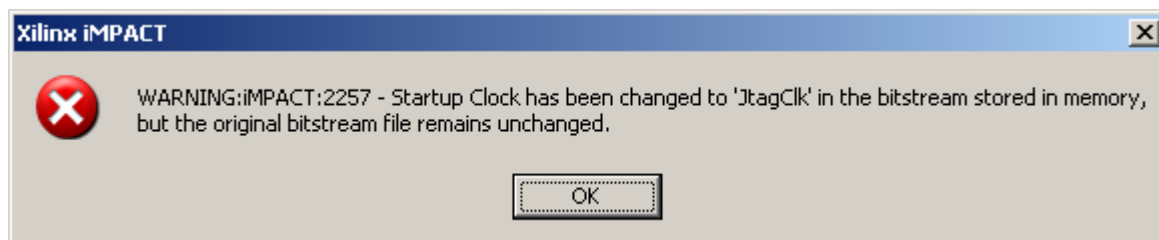
Strange Software Bug Warning: Sometimes – specifically, if the top portion of the main iMPACT window is not large enough to display the diagram of the two parts – the following file selection dialogs will not pop up automatically. If this happens, you will need to right-click on each of the two parts (the FPGA and the PROM) and select “Assign New Configuration File...” when following the next steps:

First, the FPGA should be highlighted in the main window (“xc3s200”). You should select the “**decoder.bit**” file:



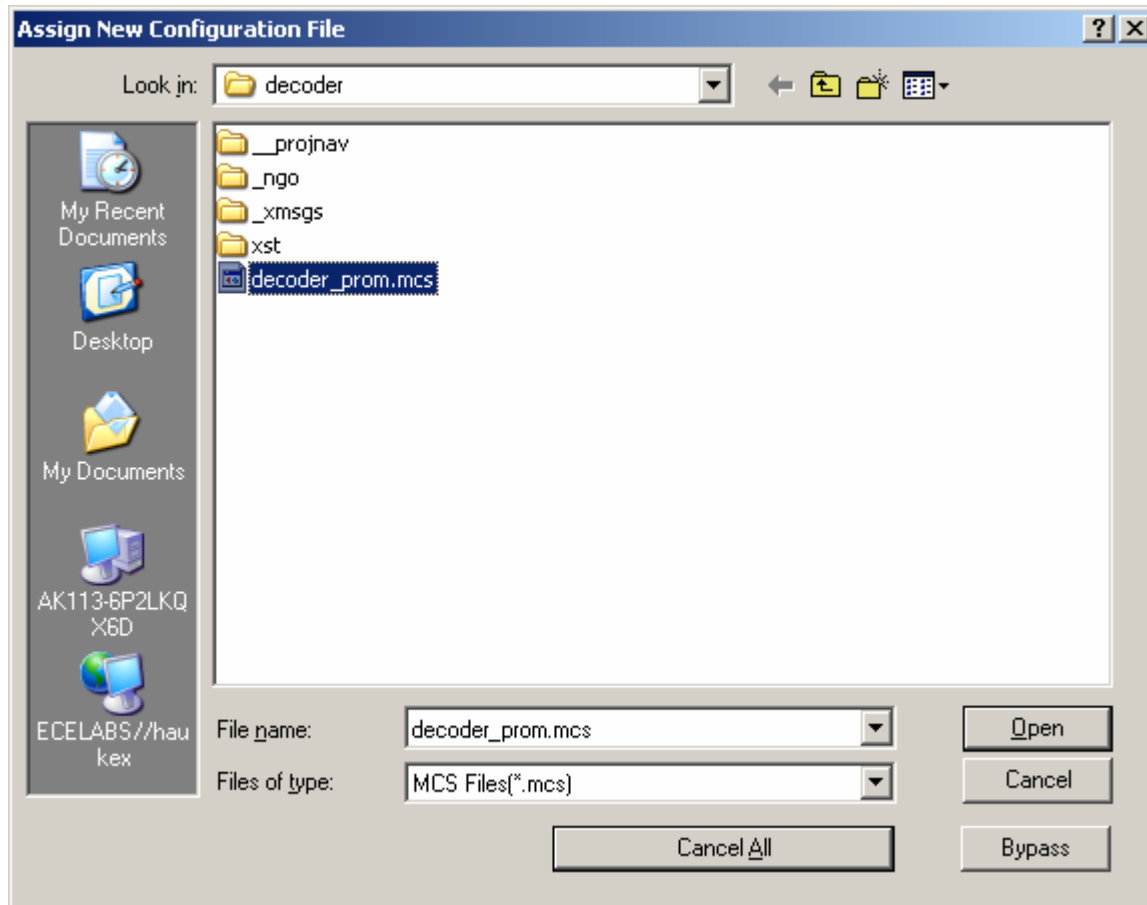
Click **Open**.

If you did not previously change the “Start-Up Clock”, you may receive this warning:



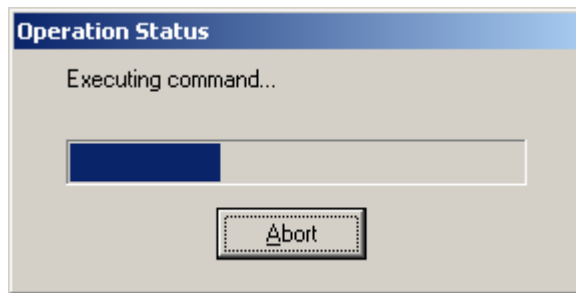
Simply click **Ok**.

The PROM should now be highlighted in the main window (“xcf02s”). If you followed the steps in Part 2, select the “**decoder_prom.bit**” file that you generated. If you skipped Part 2, click “Bypass” instead of Open.

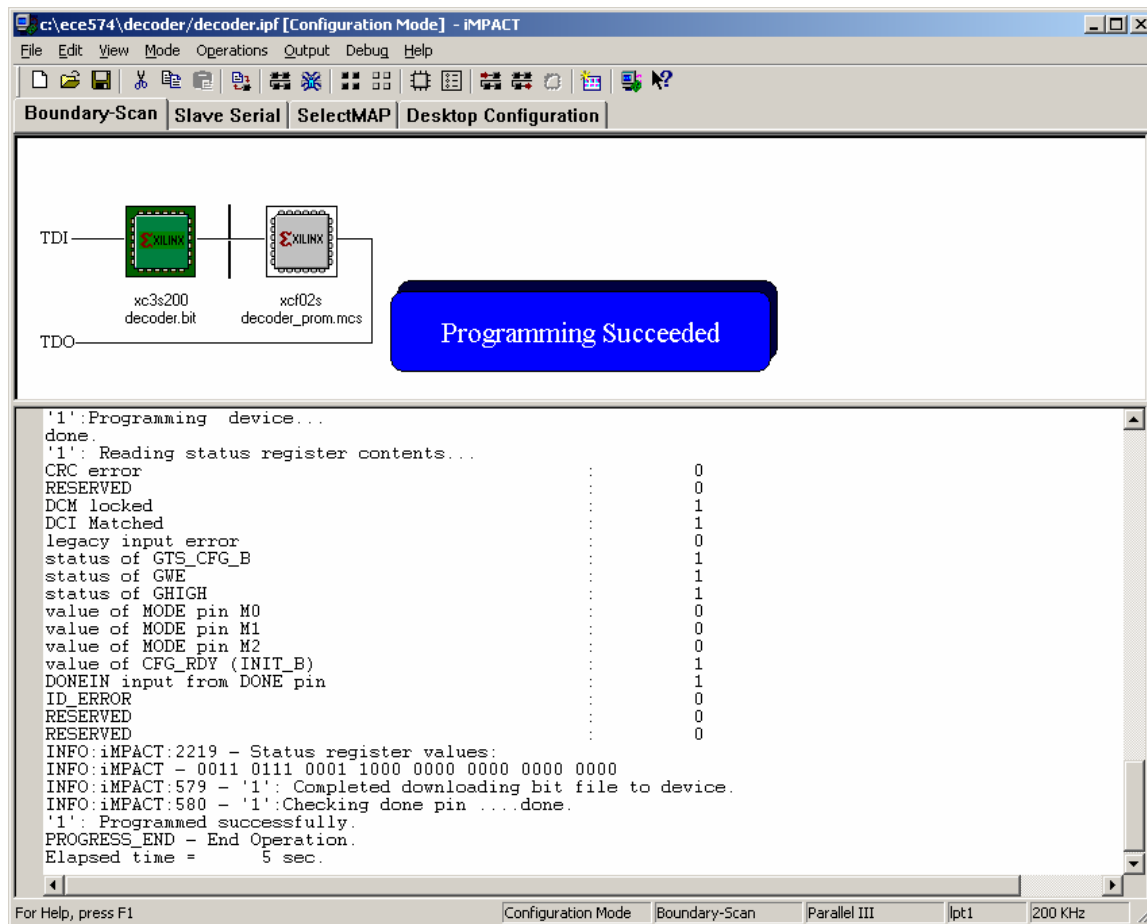


Click **Open**, or **Bypass** if you did not complete Part 2.

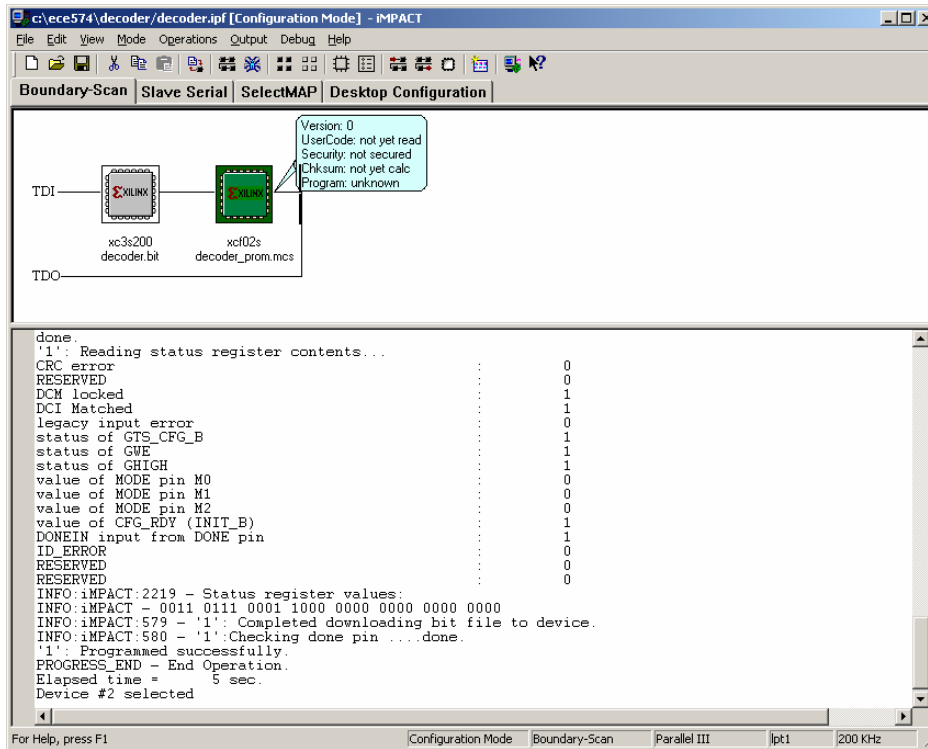
The FPGA will now be programmed:



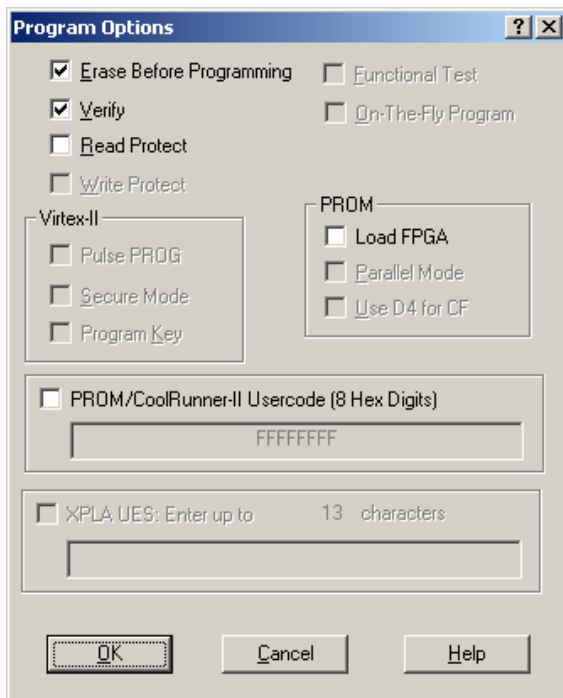
Followed by the message:



If did not follow the steps in Part 2, you can skip the following steps for programming the PROM.

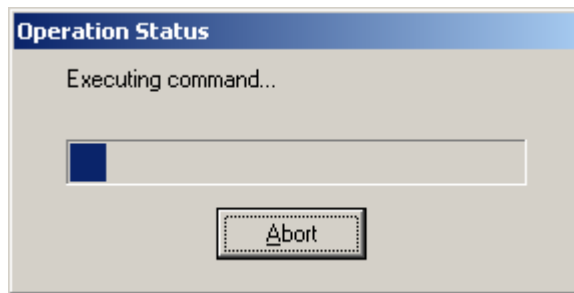


Right-click on the PROM and select “**Program**”. The following dialog will appear:

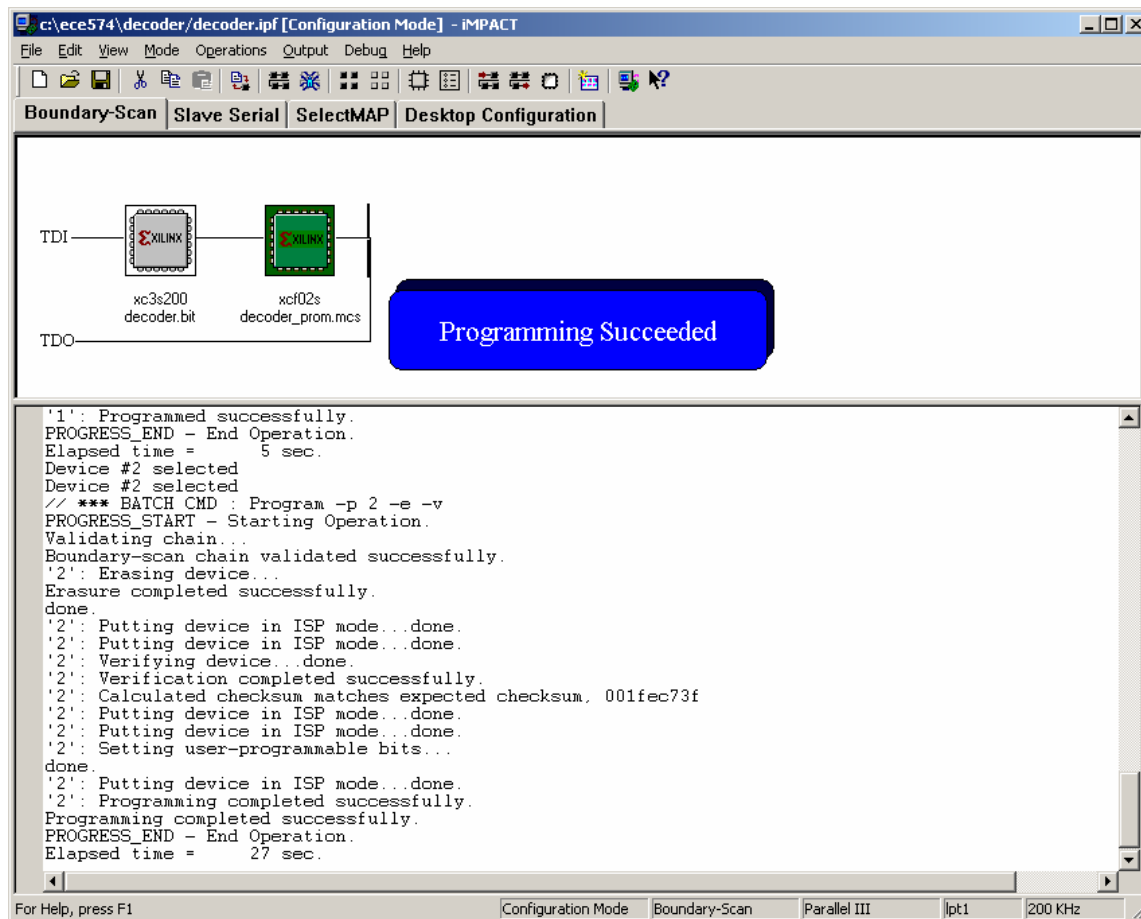


Make sure that “Erase Before Programming” and “Verify” are both checked. Then click **Ok**.

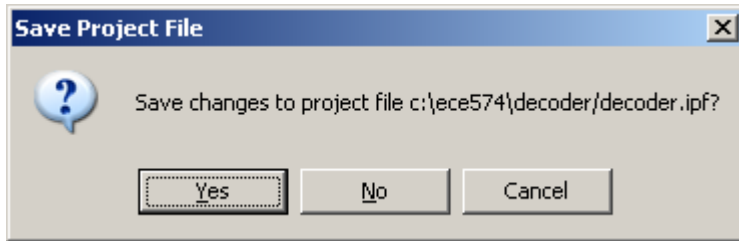
The device will be programmed:



Followed by the message:



You can now close iMPACT. You may be asked:



If you followed the steps in Part 2a above, you can select **Yes** here, *otherwise make sure to always answer No*.

If you did not follow the steps in Part 2a, and accidentally click Yes in this dialog, then whenever you double-click “Generate PROM, ACE, or JTAG File”, iMPACT will not show you the dialogs to create the PROM file as shown in Part 2. There are two workarounds to this problem: (1) delete any “*.ipf” files in the project’s directory before you try to generate a PROM file, or (2) when iMPACT opens, select File → New and select “Prepare Configuration Files”, then follow the steps as described in Part 2.