

## EE 4801: Advanced Computer System Design

### C Term 2005: HW6 (due Tuesday March 1<sup>st</sup> at 11.00 in class)

- A reminder that all homework must be completed individually.
  - No handwritten work accepted (diagrams can be neatly hand drawn)
  - **Add diagrams as necessary to help your descriptions**
  - Read section 18.1 and 18.3
  - Read sections 2.3, 11.2, 11.4, 12.4, 13.5,
  - Read sections 14.1
1. [20 marks] An SMP has two processors (P1 and P2), each with local cache. They use the MESI protocol to maintain cache coherency. Draw a block diagram of the system and show the cache contents (including MESI status) and main memory contents for the following operations (assume the caches are empty to start) :
    - P1 - Read memory location 100
    - P1 - Read memory location 101
    - P2 - Read memory location 100
    - P2 - Write memory location 102
    - P1 - Write memory location 100
    - P2 - Read memory location 100
    - P1 - write memory location 102
    - P2 - read memory location 101
  2. [20 marks] The Pentium is an example of a CISC and the Power PC is an example of a RISC.

With reference to their register sets, instruction formats, and addressing modes, show the main differences between these two types of processors.
  3. [10 marks] Instruction pipelining is used as an architectural technique on newer processors to provide performance improvements. Show an example of a 6-stage pipeline executing a sequence of instructions that includes a branch instruction.
  4. [20 marks] Draw a data dependence graph of the following instructions:
    - a.  $C = (A * 2 + B * 3) * 2 * I$
    - b.  $Z = M + (N * 2)$
    - c.  $Q = (C + A + B) - (4 * (I + J))$

Assume you have a superscalar processor with two ld/st units, two integer units, and two FPUs. How many clocks will it take to execute the three instructions above?

Assume that data is available two clock cycles after a load is completed. Two instructions have been completed (note: the FPUs can be used for integer operations).

<b>LD/ST 0</b>	<b>LD/ST 1</b>	<b>INT 0</b>	<b>INT 1</b>	<b>FPU 0</b>	<b>FPU 1</b>
LD A					
		A * 2			

5. [10 marks] Give examples of how a superscalar machine will optimize instructions for execution.
  
6. [10 marks] Briefly describe the difference between a Harvard architecture and a von Neuman architecture (this is not covered in the text book)
  
7. [10 marks] Draw a simple block diagram of the following types of computer: SISD, SIMD, MISD, MIMD