This tutorial shows how to create a simple project using a DCM (Digital Clock Manager).

The DCM generates 25MHz signals from the 100MHz xtal clock connected to the FPGA.

Create a simple module with the following ports:
Add a new IP source:

Call it dcm_25 (for 25MHz DCM)

Next and Select the Clocking Wizard core:
Click Next and then Finish.

Change the output frequency of CLK_OUT1 to 25MHz.
Click Next to go through next few pages and click Generate.

You can now see the dcm_25 in the Design pane,

Select it and you will see some options in the Processes pane.
Select the View HDL Instantiation Template

Double-click the View HDL Instantiation Template process:

```vhdl
-- The following code must appear in the VHDL architecture beside
-- Begin Out here for COMPONENT Declaration ---------

component dom_25
  port
  (  
    -- Clock in ports
    CLK_IN : in std_logic;
    -- Clock out ports
    CLK_OUT : out std_logic;
    -- Status and control signals
    RESET : in std_logic;
    LOCKED : out std_logic
  );
end component;

-- COMPONENT END --------- End COMPONENT Declaration ---------

-- The following code must appear in the VHDL architecture
-- body. Substitute your own instance name and net names.
-- Begin Out here for INSTANTIATION Template ---------

your_instance_name : dom_25
port map
  (  
    -- Clock in ports
    CLK_IN => CLK_IN,  
    -- Clock out ports
    CLK_OUT => CLK_OUT,  
    -- Status and control signals
    RESET => RESET,  
    -- INST_TAG_END --------- End INSTANTIATION Template ---------
```
Copy and Paste the DCM instantiation templates to your original VHDL:

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity DCM_example is
    Port ( fpga_clk : in STD_LOGIC;
    reset : in STD_LOGIC;
    counter_led : out STD_LOGIC;
    lock_led : out STD_LOGIC);
end DCM_example;

architecture Behavioral of DCM_example is
component dcm_25
    port
    ( 
    CLK_IN1 : in std_logic;
    CLK_OUT1 : out std_logic;
    RESET : in std_logic;
    LOCKED : out std_logic);
end component;

signal count : integer range 0 to 9;
signal clk_2SM : std_logic;
begin

    instance_name : dcm_25
    port map
    ( 
    CLK_IN1 => fpga_clk, --100MHz xtal clock to FPGA;
    CLK_OUT1 => clk_2SM, --25MHz clock for the counter;
    RESET => reset,
    LOCKED => lock_led); --light is on when DCM is locked;

    -- count from 0 to 9 with a frequency of 25MHz
    count_process: process(reset, clk_2SM)
    begin
```

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Create a UCF File

Synthesize, Implement, and Generate a Programming File.

Here is a schematic of what we have created:
Using DCMs