A 150 mW, 155 MHz Phase Locked Loop with Low Jitter VCO

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Application and Requirements

Serial data transmission over fiber optic link; requires:
- Low bit error rate (BER)
- Low cost, low power, simple interface
- Recover bit clock from serial data

Transmit end

Receive end

Clock recovery

1994 ISCAS
Clock Recovery with AD806, AD807 PLLs

Advantage
- Low cost: entire system can be integrated
- Requires integrated, low jitter VCO
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<th>SPECIFICATION</th>
<th>GOAL</th>
<th>MEASURED RESULT</th>
<th>COMMENTS</th>
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<tr>
<td>CENTER FREQUENCY $f_0$</td>
<td>155.52 MHz</td>
<td>155.5 MHz (trim)</td>
<td></td>
</tr>
<tr>
<td>TUNING RANGE</td>
<td>10 %</td>
<td>10 %</td>
<td></td>
</tr>
<tr>
<td>JITTER</td>
<td>60 ps rms</td>
<td>30 ps rms</td>
<td>Should also be insensitive to supply noise</td>
</tr>
<tr>
<td></td>
<td>0.95 % UI</td>
<td>0.5 % UI</td>
<td></td>
</tr>
<tr>
<td>LINEARITY</td>
<td>5 %</td>
<td>1 %</td>
<td>Affects closed loop parameters</td>
</tr>
<tr>
<td>TEMPERATURE DRIFT OF $f_0$</td>
<td>10 %</td>
<td>5 %</td>
<td>Stay within VCO tuning range over T</td>
</tr>
<tr>
<td>DUTY CYCLE</td>
<td>50 % ±1 %</td>
<td>50 % ±1 %</td>
<td>Important for phase detector</td>
</tr>
<tr>
<td>QUADRATURE</td>
<td>90</td>
<td>10</td>
<td>For frequency detector; not critical</td>
</tr>
<tr>
<td>TOTAL PLL POWER (5V supply)</td>
<td>140 mA</td>
<td>25 mA</td>
<td>Low capacitance of DI process (XFCB)</td>
</tr>
<tr>
<td></td>
<td>700 mW</td>
<td>125 mW</td>
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Development of Basic Design: 2 Stage Ring

Inherent 50% duty cycle

Quadrature to the extent that stage delays are matched

Control frequency by controlling stage delay
Delay Interpolator

Interpolation fraction $x$ controlled by differential $V_{CTL(dif)}$

Avoid common mode influence

Basic Ring Design

Requirements met:
- Low duty cycle distortion
- Quadrature
- Low power

Shortcomings:
- Control nonlinear
- Temperature drift
- Jitter from supply
Control Nonlinearity

Delay interpolation: Linear in time $T$
Frequency $f = 1/T$ : inherently nonlinear V-to-f
**Simulated** linearity error: 4 %
Linearity Compensation

Translinear cell with emitter area unbalance $\lambda:1$
Well controlled compensating nonlinearity

Measured Linearity

![Graph showing measured linearity]

- **Output Frequency [MHz]**
- **VCO Input [V]**
- **Linearity Error [%]**
PTAT bias: drift reduced to 5% (520 ppm/°C, end-to-end)
Jitter Increased by Supply Noise Coupling

MODEL OF POWER SUPPLY NOISE

DELAY GATE

\[ \text{V}_{\text{ripple}} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{I}_{\text{TAIL}} = \text{I}_{\text{C5}} + j\omega \text{C}_{\text{jc}} \text{V}_{\text{ripple}} \]

\[ \text{C}_{\text{jc}} \]

\[ \text{100fF} \]

\[ \text{V}_{\text{BIAS}} \]

\[ \text{V}_{\text{EE}} \]

\[ \text{V}_{\text{out}} \]

V_{\text{ripple}} \text{ couples to differential pair tail current via } \text{C}_{\text{jc}}
Reducing Delay Sensitivity to Supply Noise

MODEL OF POWER SUPPLY NOISE

DELAY GATE

DECOUPLING NETWORK

VCC

V ripple

VCC

V bias

Vee

Vout

Vin

Q4A

Q4B

Q6

Q7

CBP 1pF

RBP 10k

CjC 100nF

1994 ISCAS
Simulated Power Supply Rejection

Simulation conditions:
5V supply
0.2V p-p ripple

P-P JITTER (% UNIT INTERVAL)

1 %

0.1 %

ORIGINAL

WITH DECOUPLING NETWORK

100MHz 1GHz
RIPPLE FREQUENCY

Measurement: No bit errors at 120mV p-p @ 155 MHz
## Summary

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<th>Basic ring VCO meets some requirements</th>
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<tr>
<td>- Inherent 50% duty cycle</td>
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<td>- Adequate quadrature</td>
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<td>- Low power with XFCB</td>
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<th>Design improvements for remaining requirements</th>
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<tr>
<td>- Linearity compensation with translinear cell</td>
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<td>- PTAT bias reduces temperature drift</td>
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<td>- Decoupling network reduces supply sensitivity</td>
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**AD806**
- Low power, low jitter (45 ps rms), 155MHz PLL
- Input sensitivity 2mV with on-chip comparator

**AD807**
- AD806 with loss-of-signal detection
- Lower jitter: 30 ps rms