SMALL SIGNAL (AC) MODEL OF 2 STAGE OP-AMP

\[ V_{DD} \]

\[ \begin{align*}
M_3 & \quad M_4 \\
M_5 & \quad V_g5 \\
C_C & \quad V_{out}
\end{align*} \]

\[ M_6 \quad M_7 \quad M_8 \]

\[ \text{M}_5 \quad \text{M}_8 \]

\[ \text{M}_3 \quad \text{M}_4 \text{ MIRROR} \]

\[ V_{id} \]

\[ \begin{align*}
G_mV_{id} & \quad R_{o2}R_{o4} \\
& \quad \frac{(1+A_2)C_C}{G_{ms}V_g5} \\
& \quad R_{o5}R_{o8} \quad V_{out} \quad C_L
\end{align*} \]

\[ V_{DD} \rightarrow \text{small signal ground} \]

\[ \text{DOMINANT POLE} \quad \frac{1}{2\pi RC} \]

\[ \frac{1}{2\pi \left( R_{o2}R_{o4} \right) \left( 1+A_2 \right) C_C} \]

\[ \frac{1}{2\pi \left( R_{o5}R_{o8} \right) C_L} \]

[Diagram showing \( C_{eq} = (1+A_2)C_C \)]

[Diagram showing Miller says EQUIV]
COMPLETE TRANSFER FUNCTION

UNITY GAIN (0 dB)

DOMINANT POLE

FOR MOST TRANSFER FUNCTIONS:
RANGE OF FREQUENCY BETWEEN POLES

POLE TERMS \((1 + j \frac{f}{f_p})\) MAG \(\approx \frac{1}{f / f_{p1}}\) OR

For the transfer function:

\[
A(f) = \frac{A_o}{(1 + j \frac{f}{f_{p1}})(1 + j \frac{f}{f_{p2}})}
\]

MAGNITUDE

\[
|A(f)| = \frac{A_o}{\sqrt{1 + (\frac{f}{f_{p1}})^2} \sqrt{1 + (\frac{f}{f_{p2}})^2}}
\]

Approximate

\[
|A(f)| \approx \frac{A_o}{\left(\frac{f}{f_{p1}}\right)} (1)
\]

Finally \(f_T\)

\[
1 = \frac{A_o}{f_T / f_{p1}}
\]
\[ 1 = \frac{g_{m_1} \left( \frac{\theta_2}{\theta_4} \right) A_2}{f_T} \cdot \frac{1}{1 - \frac{2\pi f_T}{2\pi \left( \frac{\theta_2}{\theta_4} \right) (\pi A_2) C_c}} \Rightarrow f_T = \frac{g_{m_1}}{2\pi C_c} \]

\[ A_2 \gg 1 \]
2-Stage Op-Amp Phase Margin vs. $C_{LOAD}$

- $C_{LOAD} = 10pF, 100pF, 1000pF$
- Phase margin $\phi_M$ degrades as $C_{LOAD}$ increases
1-Stage ("gm-C" "transconductor") Op-Amp

**ALL OTHER NODES IN SIGNAL PATH DIODE CONNECTED MOSFETs IMPEDANCE \( \approx \frac{1}{g_m} \approx 1 \text{K}\Omega \)**

\( I_{\text{BIAS}} - \frac{g_{\text{mVid}}}{2} \)

\( I_{\text{BIAS}} + \frac{g_{\text{mVid}}}{2} \)

\( 8 \left( \frac{I_{\text{BIAS}} + g_{\text{mVid}}}{2} \right) \)

\( 8 \left( \frac{I_{\text{BIAS}} - g_{\text{mVid}}}{2} \right) \)

**Vout IS THE ONLY HIGH IMPEDANCE NODE**

\( \frac{R_{\text{on}}}{R_{\text{op}}} \approx 100 \text{K}\Omega \)

**INHERENTLY 1 POLE OP-AMP**

- Only one high impedance node: \( C_{\text{LOAD}} \) compensates
1-Stage ("gm-C" "transconductor") Op-Amp

\[ C_{LOAD} = 1000\text{pF}, 10000\text{pF}: \phi_M \text{ same as } C_{LOAD} \uparrow \]

- Unity gain frequency \( f_T \) worse, but always stable
1-Stage Problem

- Lousy DC gain $\approx 90$ (39 dB)
- Solution: Add cascode to high impedance node
1-Stage with Cascodes

CASCODE CURRENT MIRROR

* PMOS CASCODING DEVICES

VBIAS P

DIFF PAIR BIAS

DIFF PAIR

* NMOS CASCODES

VBIAS N BIAS V?

HIGHER Rout DUE TO CASCODES (vgsRo HIGHER)
1-Stage with Cascodes

- $C_{LOAD} = 1000\text{pF}, 10000\text{pF}: \phi_M$ same as $C_{LOAD} \uparrow$
- Unity gain frequency $f_T$ worse, but always stable
CASCODE OP-AMP

Start with your previous op-amp, compensated. Hook it up for an inverting gain of 100. Use a 10mV input sine wave at 100Hz to get an output swing of around 1V.

The nice thing about doing it this way is you can look directly at the signal at the - input, which is close to ground, and view it up close on the scope: since there's no DC component, expanding to the max scale will not shoot the signal off the screen.

Without the cascode, your open loop gain of about 1000 should give a 1mV sine wave at the - input. With the scope probe on 1X and the scope on 2mV/division, you should be able to (barely) see a signal at the - input. Record the signal amplitude as best you can, then do the cascode as indicated below:
To cascode the internal node, you'll need a fourth CD4007 chip. Connect it as shown here:

Now when you operate the op-amp, you should see a much smaller signal amplitude at the input, corresponding to a larger open-loop gain (same output swing for a smaller input swing). The signal swing at the input will probably be too small for you to actually calculate a gain - just verifying that gain is improved is good enough.

Note: the values in the 30kΩ / 20kΩ voltage divider were chosen to set the bias rail for the cascoding devices so that all devices were in the active region. For your device parameters, it may be necessary to adjust the voltage somewhat. You can always probe the DC bias levels to establish that all devices are in the active region.
ECE4902 Lecture 12

2-Stage Op-Amp
   CL, Phase Margin Issue

1-stage op-amp
   Johns & Martin 6.2
   Improving Performance:
   Cascode

Optional Lab circuits
   Cascode Op-Amp
   Bandgap Voltage Reference
   Phase-Locked Loop

Hand In:
HW 5

Handout:
Op-Amp Slides
Cascode Op-Amp
Bandgap Voltage Reference
   Principle
   Circuit
Phase-Locked Loop

ISSUE: R{\text{BIAS}} WE HAVE BEEN USING

CAN CHANGE! DIRECTLY AFFECTS
I{\text{BIAS}}

I{\text{BIAS}} = \frac{(V_{DD} - V_{SS}) - V_{GS}}{R_{BIAS}}

I{\text{BIAS}} \rightarrow \text{SLEW RATE}

\text{g}_n \rightarrow f_T

\text{WANT THESE TO BE INSENSITIVE TO SUPPLY} (V_{DD}, V_{SS}) \text{ VARIATIONS!}
$V_{GO} = V_{BE} + PTAT$

**Figure 6.** Typical base-to-emitter voltage characteristic vs temperature for each transistor.

- **VBE**
  - Too much
  - "Just right"
  - Too little

- **PTAT**
  - Proportional to absolute temperature
  - "CTAT" (Complementary to absolute temperature)

- **VGO**
  - "Bandgap voltage of silicon"
  - [see ECE 4904]

- **VBE**
  - Extrapolate $V_{BE}$ vs temperature back to $T = 0\,^\circ\,K$ (absolute zero)

- **Ic**
  - $V_N^+ = I_E \approx I_C$

- **TC**
  - $T = 0\,^\circ\,K$ (absolute zero)
BJT:

\[ I_c = I_s \left( \frac{V_{BE}}{V_T} \right) \]

\[ \approx 0.7 V \]

SOLVE FOR \( V_{BE} \):

\[ V_{BE} = V_T \ln \left( \frac{I_c}{I_s} \right) \]

\[ V_{BE} = \frac{kT}{q} \left[ \ln \left( \frac{I_c}{I_s} \right) \right] \]

**Scale Factor**

- Proportional to emitter area of BJT
- Doubles every 10°C

**Thermal Voltage**

- Boltzmann's constant \( \frac{kT}{q} \)
- Charge \( q \)
- \( T \) in Kelvin

\[ \approx 26 \text{ mV at } T = 300 \text{ K} \]
BANDGAP VOLTAGE REFERENCE

Q₁, Q₂ BJTS:

\[ V_{BE2} = \frac{kT}{q} \ln \left( \frac{I_{C2}}{I_{B2}} \right) \]
\[ V_{BE1} = \frac{kT}{q} \ln \left( \frac{I_{C1}}{I_{S1}} \right) \]

Look at \( \Delta V_{BE} = V_{BE1} - V_{BE2} \)

\[ \Delta V_{BE} = \frac{kT}{q} \ln \left[ \frac{I_{C1}}{I_{S1}} \right] - \ln \left( \frac{I_{C2}}{I_{S2}} \right) \]

\[ \ln x - \ln y = \ln \frac{x}{y} \]

\[ \Delta V_{BE} = \frac{kT}{q} \ln \left[ \frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}} \right] \]

Mirror: \( I_{C1} = 2I_{C2} \)
\( I_{S2} = 4I_{S1} \)

Emitter areas:

\[ \Delta V_{BE} = \frac{kT}{q} \ln \left[ \frac{2I_{C2}}{4I_{S1}} \right] = \ln(8) \frac{kT}{q} \]

\[ \Delta V_{BE} = \left[ \ln(8) \frac{kT}{q} \right] T \]

\( \Delta V_{BE} \) IS PTAT!

PTAT

\[ V_{BG} = V_{BE1} + \frac{2R_2}{R_1} \Delta V_{BE} \]

Choose \( R_2, R_1 \) to get correct amount of PTAT

KVL TO \( V_{BG} \) NODE: \( V_{BG} = V_{BE1} + I_{C1} R_2 \)

\[ 2I_{C2} \]

\[ \Delta V_{BE} \] (Mirror)

\[ \Delta V_{BE} \] (Op-amp, Ohm's Law)

\[ V_{BG} = V_{BE1} + \frac{2R_2}{R_1} \Delta V_{BE} \]

4BJTS IN PARALLEL

4x Emitter AREA

4 BJTS IN PARALLEL

4x Emitter AREA
PLL

This is the most complicated of the three optional labs - but is definitely the coolest system and if you can get it working, you should be able to learn a lot.

The top level block diagram of the PLL is shown below: