PLL

This is the most complicated of the three optional labs - but is definitely the coolest system and if you can get it working, you should be able to learn a lot.

The top level block diagram of the PLL is shown below:
BUILDING THE SYSTEM — VOLTAGE CONTROLLED OSCILLATOR

The first step is to build the VCO block by itself and verify its operation:

- PMOS
  - $V_{CTL} \downarrow \Rightarrow R \downarrow$

- $V_{CTL}$ and $R$ control $f$ for LM555
  - $f \propto \frac{1}{RC}$

- $V_{CTL} \downarrow \Rightarrow R \downarrow \Rightarrow f \uparrow$

- $f_0$ "CENTER FREQUENCY"
  - "FREE RUNNING FREQUENCY" FREQ WITH ZERO INPUT

- $f_0 = f_{00} + K_{VCO} V_{CTL}$

- Slope $K_{VCO}$ [Hz/V]
Next build the PFD: "Phase/Frequency Detector"

MAKE VCO↓ WHEN ACTIVE

WHEN BOTH UP, DOWN ACTIVE: RESET BOTH TO LOOP FILTER

MAKE VCO↑

JUST COMPARE EDGES \( \phi = 0 \)

INPUT WITH MORE EDGES: OUTPUT ASSERTED MORE OFTEN

TOO FAST

SLOW DOWN

TOO SLOW

SPEED UP

UP

DOWN

PULSES
FINALLY: THE LOOP FILTER

2 INPUTS TO INTEGRATOR

AVG: PULSES BECOME CURRENTS
INTEGRATE ON $C_J$

INACTIVE: NO CURRENT INTEGRATOR

$V_{UP}$ $\rightarrow$ $+5V$

$V_{DOWN}$ $\rightarrow$ $0V$

CD4007

FOR LOOP STABILITY (CONTROLS)

CMOS INVERTER

HIGH GAIN AT TRANSITION

INTEGRATOR:

1. SMOOTH PULSES
2. ZERO STEADY-STATE ERROR (CONTROLS)

$V_{CTL}$
Making Clocks Equal?

V_IN → VCCL

V_CLK1

V_CLK2

V_CTL

FM Demodulation!

PLL forces Φ₁, Φ₂ to be equal

Edge times (φ) not affected by noise

VCTRL

PFD

REFCLK

VCOCLK

UP

DOWN

VCTRL

MUST BE SAME AS VIN!
NEED 1 GHz ON CHIP

\[ f_{\text{DIVCLK}} = \left(\frac{1}{N}\right) f_{\text{VCOCLK}} \]

\[ f_{\text{IN}} = f_{\text{VCOCLK}} = N f_{\text{IN}} \]