ECE4902 Lecture 9

2-Stage Op-Amp
  1st-2nd Stage: NMOS or PMOS?!
  DC Analysis
  Input Common-Mode Range
  Feedback
  Stability

Handout:
Lab 8/9 Op-amp (2X)
Lab 8/9 Review Slides

MOST IMPORTANT LECTURE OF YOUR LIFE

ECE4902
DC OUTPUT

V_{DS3} = V_{GS3}
(DIODE CONNECTED FOR MIRROR)

1st STAGE OUTPUT DC BIAS

\[ I_{D1} = I_{D2} \]

2nd STAGE INPUT DC BIAS

\[ g_m = \frac{2I_D}{V_{GS} - V_{TH}} \]

BAD NEWS

SMALL 7V BIG!

V_{DS} > V_{GS} - V_{TH}

V_{OUT} \text{ TRIODE CRASH FOR } V_{OUT} \leq +2V! ?

NMOS OR PMOS?

\[ V_{DD} = +5V \]

\[ V_{SS} = -5V \]

\[ V_{DS} \approx 2V \]

\[ V_{GS} \approx 2V \]

\[ V_{GS} = +8V \]

\[ V_{TH} = +1V \]

\[ V_{GS} - V_{TH} \]

\[ V_{OUT} \]

\[ +3V \text{ DC BIAS} \]

\[ -5V \]

ACTIVE LOAD
CD4007: * MOSFETS ARE SAME SIZE: SAME $I_D$

IN PRACTICE: SIZE $M_6, M_7, M_8$ TO SCALE $I_D$ DIFFERENTLY
(USUALLY MORE $I_D$ FOR OUTPUT STAGE)
Op-amp input common mode (CM) range limits: **NEED TO HAVE ALL DEVICES IN SATURATION**

1. TRIODE CRASH, M7 (I\text{BIAS} DECREASES)
2. V\text{DS7} = V\text{ICM} - V\text{GS1}
3. V\text{ICM} - V\text{GS1} + V\text{DS1} + V\text{SG3} = V\text{DD}
4. M1 TRIODE CRASH
5. M1, M2 NO LONGER IN SAME OP REGION
DC OPERATING CONDITION?

FIND ALL VGS, I0, NODE VOLTAGES

ASSUME ALL DEVICES IN ACTIVE REGION

START WITH I_B (OHM'S LAW)

\[
\frac{V_{DD} - (V_{SS} - V_{GS6})}{150k\Omega} = I_B = \frac{+5V - (-2.5V)}{150k\Omega} = 50mA = I_{D6}, I_{D7}, I_{D8} \quad \text{GUESSED 2.5V}
\]

REASONABLE? SQUARE LAW: 50mA = \( \frac{2.6E-5}{2} \times \frac{350}{10} \times (V_{GS6} - 1.9)^2 \) \Rightarrow V_{GS6} = 2.23V

DIFF PAIR: SYMMETRY: I_{D1} = I_{D2} = 25mA

V_{GS1}, V_{GS2} SQ LAW: 25mA = \( \frac{2.6E-5}{2} \times \frac{350}{10} \times (V_{GS1} - 1.9)^2 \) \Rightarrow V_{GS1,2} = 2.13V

M3, M4 MIRROR LOAD: I_{D3}, I_{D4} = 25mA

V_{GS3}, V_{GS4} SQ LAW: 25mA = \( \frac{9.1E-6}{2} \times \frac{900}{10} \times (V_{GS3} - (-1.6V))^2 \) \Rightarrow V_{GS3,4} = -1.85V

M5: 50mA SET BY M8 LOAD

SQ LAW: 50mA = \( \frac{9.1E-6}{2} \times \frac{900}{10} \times (V_{GS5} - (-1.9V))^2 \) \Rightarrow V_{GS5} = -1.9V

All PMOS = 900

NMOS = 350

\[ \text{\underline{Units}} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N-channel</th>
<th>P-channel</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{TH}</td>
<td>+1.90</td>
<td>-1.60</td>
<td>V</td>
</tr>
<tr>
<td>( \mu C_{os} )</td>
<td>2.6E-5</td>
<td>9.1E-6</td>
<td>A/V^2</td>
</tr>
<tr>
<td>( \lambda ) (L=10\mu m)</td>
<td>0.05</td>
<td>0.028</td>
<td>V^-1</td>
</tr>
</tbody>
</table>
Studio 8 & 9 Review

• Operational Amplifier
  – Stability
  – Compensation
  – Miller Effect
  – Phase Margin
  – Unity Gain Frequency ✓
  – Slew Rate Limiting ✓

• Reading: Razavi ch. 9, 10
  – Lab 8, 9 op-amp is Fig. 10.34 in sec. 10.5.1
  – (see also Johns & Martin sec 5.2 pp. 232-242)
Two-stage op-amp

V_{DD} = +5V

MIRROR 1st → 2nd

CS AMPL

DIFF PAIR

DC Bias

V_{out}

V_{SS} = -5V

All P: \frac{900}{10}

All N: \frac{350}{10}

150k\Omega

50\mu A
Analysis Strategy

- Recognize sub-blocks
- Represent as cascade of simple stages

![Circuit Diagram]

- All P: $\frac{900}{10}$
- All N: $\frac{350}{10}$

V_{DD} = +5V

V_{SS} = -5V

$V_{out}$

M3, M4, M5, M6, M7, M8

$V_{G6}$

50μA
Total op-amp model

Input differential pair    Common source stage

\[ g_{m1} = \frac{2I_{D1}}{V_{G51} - V_{TH1}} \]
\[ r_{O2} = \frac{1}{\lambda I_{O2}} \]
\[ g_{m5} = \frac{2I_{DS}}{V_{G55} - V_{TH5}} \]
## DC operating point

<table>
<thead>
<tr>
<th></th>
<th>$I_D[\mu A]$</th>
<th>$V_{GS-V_{TH}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>25</td>
<td>0.235</td>
</tr>
<tr>
<td>M2</td>
<td>25</td>
<td>0.235</td>
</tr>
<tr>
<td>M3</td>
<td>25</td>
<td>0.247</td>
</tr>
<tr>
<td>M4</td>
<td>25</td>
<td>0.247</td>
</tr>
<tr>
<td>M5</td>
<td>50</td>
<td>0.350</td>
</tr>
<tr>
<td>M6</td>
<td>50</td>
<td>0.332</td>
</tr>
<tr>
<td>M7</td>
<td>50</td>
<td>0.332</td>
</tr>
<tr>
<td>M8</td>
<td>50</td>
<td>0.332</td>
</tr>
</tbody>
</table>
### Small signal parameters

<table>
<thead>
<tr>
<th></th>
<th>$I_D[\mu A]$</th>
<th>$V_{GS-V_{TH}}$</th>
<th>$g_m[\mu A/V]$</th>
<th>$r_O$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>25</td>
<td>0.235</td>
<td>208</td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td>25</td>
<td>0.235</td>
<td></td>
<td>800kΩ</td>
</tr>
<tr>
<td>M3</td>
<td>25</td>
<td>0.247</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M4</td>
<td>25</td>
<td>0.247</td>
<td></td>
<td>1.43MΩ</td>
</tr>
<tr>
<td>M5</td>
<td>50</td>
<td>0.350</td>
<td>285</td>
<td>715kΩ</td>
</tr>
<tr>
<td>M6</td>
<td>50</td>
<td>0.332</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M7</td>
<td>50</td>
<td>0.332</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M8</td>
<td>50</td>
<td>0.332</td>
<td></td>
<td>400kΩ</td>
</tr>
</tbody>
</table>

Note: $\lambda_n = 0.050 \frac{V}{\Omega}$; $\lambda_p = 0.028 \frac{V}{\Omega}$
Total op-amp model: Low frequency gain

Input differential pair  Common source stage

\[ a_{v1} = g_{m1}(r_{O2}\|r_{O4}) \]
\[ a_{v1} = (208 \mu A/V)(800k\Omega\|1.43M\Omega) \]
\[ a_{v1} = 106 \]

\[ a_{v2} = g_{m2}(r_{O5}\|r_{O8}) \]
\[ a_{v2} = (285 \mu A/V)(400k\Omega\|715k\Omega) \]
\[ a_{v2} = 73 \]

\[ \frac{V_{out}^+}{V_{in}} \cong 7000 \]
Total op-amp model with capacitances

Gate of M5

Load: scope probe ≈ 10pF

\[ C_g = (900 \, \mu m)(10 \, \mu m) \left( 4.17E - 4 \frac{F}{m^2} \right) \]

\[ C_g = 3.74 \, pF \]

Each cap will contribute 1 pole to \( \frac{V_{out}}{V_{in}} \) (f)

Only 2 high impedance nodes: \( V_{g5}, V_{out} \)
Total op-amp model with capacitances

**First stage pole**

\[ f_{p1} = \frac{1}{2\pi \left( r_{O2} || r_{O4} \right) C_{g5}} \]

\[ f_{p1} = \frac{1}{2\pi \left( 800k\Omega || 1.43M\Omega \right) \left( 3.74pF \right)} \]

\[ f_{p1} = 82kHz \]

**Second stage pole**

\[ f_{p1} = \frac{1}{2\pi \left( r_{O5} || r_{O8} \right) C_L} \]

\[ f_{p1} = \frac{1}{2\pi \left( 400k\Omega || 715k\Omega \right) \left( 10pF \right)} \]

\[ f_{p1} = 61kHz \]
Open loop transfer function

- Product of individual stage transfer functions
  \[
  A(j\omega) = \frac{g_{m1}(r_{O2} || r_{O4}) g_{m5}(r_{O5} || r_{O8})}{1 + j\omega(r_{O2} || r_{O4}) C_{g5} [1 + j\omega(r_{O5} || r_{O8}) C_L]}
  \]

- Numerically (using \( \omega = 2\pi f \))
  \[
  A(j\omega) = \frac{7738}{1 + j\left(\frac{f}{82\text{kHz}}\right)} [1 + j\left(\frac{f}{61\text{kHz}}\right)]
  \]

- Check Bode plot simulation; predicts:
  - DC gain = 20\log(7738) = +78dB
  - Unity gain frequency \( \sim 6.2 \text{ MHz} \)
Two-stage op-amp: Simulation Schematic

---

C_L = 10 pF

only parasitics
DC Operating Point Simulation

DC Response

CAUTION: IF DO AC SIM WITH
V_{IN} = 0 OPERATING
POINT WILL SHOW LOW
OPEN LOOP GAIN

OP POINT: 2.885 mV

IDEAL

Systematic Offset!

A: (2.11783m -3.81929) delta: (1.39772m 7.02858)
B: (3.51555m 3.20929) slope: 5.02861K

OK: A_0 JUST \( \leq 5000 \) \( \Rightarrow \) 7800
NEEDS TO BE LARGE! \( \geq 30\% \) ERR M!?
Bode plot

- Magnitude, phase on log scales
- Pole: Root of denominator polynomial
Open loop Bode plot

- Product of terms: Sum on log-log plot

\[ 20 \log |A| \]

DC GAIN \( A_0 \)

-20 dB/dec

-40 dB/dec

\[ \omega \]

\[ \omega \]

\[ -90^\circ \]

\[ -180^\circ \]
Open Loop Bode Plot Simulation

Note: AC source at input also needs DC component to account for systematic offset!
Check Open Loop Bode Plot Simulation

\[ \sqrt{\text{DC gain}} \sim +78\text{dB} \]

Unity gain \sim 16\text{MHz}
Stability example: Closed loop follower

- **Negative feedback:**
  Output connected to inverting input

- **Gain should be ~ 1**

\[
\begin{align*}
v_{\text{out}} &= A(v_{\text{in}} - v_{\text{out}}) \\
v_{\text{out}}(A + 1) &= A v_{\text{in}} \\
v_{\text{out}} &= \left(\frac{A}{A + 1}\right) v_{\text{in}} \\
&\approx 1 \text{ as } A \gg 1
\end{align*}
\]
Unity gain: Why bother?

\[ v_{out} = \left( \frac{R_L}{R_L + R_S} \right) v_{in} \]

- **No buffer:**
  - Voltage divider
  - Signal reduced due to voltage drop across \( R_S \)

- **With buffer:**
  - No current required from source
Lab 9 Problem: Instability

- Oscillation superimposed on desired output!??

$\nu_{IN}$

$\nu_{OUT}$
Lab 9 Problem: Instability

- Ground $v_{in}$: Output for zero input?!?
- Why? Need...

![Graph showing oscillation](image-url)

For this waveform, $\frac{V_{out}}{V_{in}} = \infty$
Controls: ES3011 in 20 minutes

- General framework
  A: Forward Gain
  $\beta$: Feedback Factor Factor
  fraction of output fed back to input

![Diagram](image)
Example: Op-amp, Noninverting Gain

**A: Forward Gain**

Op-amp open loop gain

\[ V_{out} = A(V_+ - V_-) \]

Transfer function \( A(j\omega) \)

\[ \beta: \text{Feedback Factor} \]

\[ \beta = \frac{R_1}{R_1 + R_2} \]
Closed Loop Gain

- **Output**
  \[ v_{out} = A(v_{in} - (\beta v_{out})) \]

- **Solve for** \( v_{out} / v_{in} \)
  \[ v_{out} = A v_{in} - A \beta v_{out} \]
  \[ (1 + A \beta) v_{out} = A v_{in} \]
  \[ \frac{v_{out}}{v_{in}} = \frac{A}{1 + A \beta} \]
Op-amp with negative feedback

- If $A\beta \gg 1$
  \[
  \frac{v_{out}}{v_{in}} = \frac{A}{1 + A\beta} \approx \frac{A}{A\beta} \quad \Rightarrow \quad \frac{v_{out}}{v_{in}} \approx \frac{1}{\beta}
  \]

- Closed loop gain determined only by $\beta$

- Advantage of negative feedback:
  Open loop gain $A$ can be ugly (nonlinear, poorly controlled) as long as it's large!
Example: Op-amp, Noninverting Gain

$\beta$: Feedback Factor

$$\beta = \frac{R_1}{R_1 + R_2}$$

Closed loop gain

$$\frac{v_{out}}{v_{in}} = \frac{R_1 + R_2}{R_1} = \frac{1}{\beta}$$
Reexamine closed loop transfer function

• Output with no input: infinite gain
• Infinite when $1 + A\beta = 0$
• Condition for oscillation:
  $$1 + A\beta = 0$$
• In general $A, \beta$ functions of $\omega$
• If there's a frequency $\omega$ at which $1 + A\beta = 0$: Oscillation at that frequency!

$$\frac{v_{out}}{v_{in}} = \frac{A}{1 + A\beta} \delta$$
Example: follower

\[ \beta = 1 \quad \rightarrow \quad \frac{v_{out}}{v_{in}} = \frac{A}{1 + A} \]

- Use \( A(j\omega) \), solve for \( 1 + A = 0 \)
- No thanks!

\[ A(j\omega) = \frac{g_{m1}(r_{o2}||r_{o4})g_{m5}(r_{o5}||r_{o8})}{1 + j\omega(r_{o2}||r_{o4})C_{g5}} \left[ 1 + j\omega(r_{o5}||r_{o8})C_L \right] \]
Reexamine condition for oscillation

\[ 1 + A\beta = 0 \rightarrow A\beta = -1 \]

Magnitude and phase condition:
\[ |A\beta| = 1 \quad \text{AND} \quad \angle A\beta = -180^\circ \]

- Easier to get from Bode plot
Look at original $A\beta$ for 2 stage op-amp

- Find $\omega$ at which $|A\beta| = 1$; Check $\angle A\beta = -180^\circ$?

Trouble!
Simulation Aβ for 2 stage op-amp

Unity loop gain at ~ 16MHz

> 180° phase lag at unity loop gain!

- Causes closed-loop instability
Compensation: “Dominant Pole”

- Move one pole to lower frequency
- How?

Move unity loop gain frequency $f_T$ to lower value

So accumulated phase lag at $f_T$ hasn’t reached -180°
Compensation: “Dominant Pole”

- Need to increase capacitance by $\approx 1000X$:
  BAD! Die area cost
Miller Effect

- Impedance across inverting gain stage $G$
- Reduced by factor equal to $(1+G)$

For high speed amp: BAD

\[ \frac{1}{C(1+G)} \text{ looks bigger} \]
Math for Miller effect

\[ i_x = \frac{v_x - (-Gv_x)}{Z} \]

\[ i_x = \frac{v_x(1 + G)}{Z} \]

\[ \frac{v_x}{i_x} = Z_{in} = \frac{Z}{(1 + G)} \]

- Impedance across inverting gain stage G
- Reduced by factor equal to \((1+G)\)
Example: Impedance is capacitive

- Capacitance multiplied by (1+G)

\[ Z_{in} = \frac{Z}{(1 + G)} \]

\[ Z = \frac{1}{sC} \implies Z_{in} = \frac{1}{s(1 + G)C_{eq}} \]

- Equivalent capacitance higher by factor 1+G
- Problem for high bandwidth amplifiers
- Opportunity for compensation ...
Miller Compensation

• Need effect of large capacitance
• Use Miller effect to multiply small on-chip capacitance to higher effective value
• Effect of large capacitance without die area cost of large capacitance

save $
New schematic

- Add $C_C$ across 2nd stage

"Compensation capacitor"
New loop gain transfer function

Unity loop gain at ~65kHz

125° phase lag at unity loop gain

First pole much lower!

Unity gain freq also much lower

A: (84.359K, 134328)
B: (83.483K, -125.174)
delta: (-875.82, -128.519)
slope: 148.741m
New step response

- No oscillation!
New step response with $C_C$

- Zoom in on small-signal step response: Some overshoot and ringing
Reason: RHP zero in complete transfer function

Effect of RHP zero: additional phase lag

Open loop gain $A$ with only 2 poles

Complete transfer function looks like:

$$A(j\omega) = \frac{A_0 \left[1 - j(\omega/\omega_z)\right]}{\left[1 + j(\omega/\omega_{p1})\right]\left[1 + j(\omega/\omega_{p2})\right]}$$

See Razavi 10.5, Johns & Martin 5.2
"Phase margin"

- How stable is new transfer function?
- Phase margin = Phase lag at $|A\beta| = 1$ minus ($-180^\circ$)
- Usually want at least $60^\circ$ for stable step response
Phase margin of op-amp with $C_c$

Unity loop gain at ~65kHz

125° phase lag at unity loop gain

Phase margin = 55°
Solution to RHP zero problem

- Add $R_Z$ in series with $C_C$
- Moves RHP zero to much higher frequency
New step response with $R_Z, C_C$

- Zoom in on small-signal step response:
  No overshoot, ringing: phase margin improved
Large signal step response

- Slew Rate Limiting!??

See Solomon op-amp paper for model; rising/falling asymmetry
Dominant pole op-amp model

- Simpler model with dominant pole from $C_C$
Approximate dominant pole transfer function

\[ (1 + A_2)C_c = C_{eq} \]

\[ A(j\omega) \approx \frac{g_{m1}(r_{o2}||r_{o4})A_2}{1 + j\omega(r_{o2}||r_{o4})A_2C_c} \]

\[ A_2 = g_{m5}(r_{o5}||r_{o8}) \]

2nd stage gain

Miller multiplied \( C_c \)
Unity gain frequency

• Depends only on
  – Input stage transconductance $g_{m1}$
  – Compensation capacitor $C_C$

\[
|A(j\omega)| \approx \frac{g_{m1}(r_{o2}r_{o4})A_2}{\omega(r_{o2}r_{o4}A_2C_C)} \geq 1
\]

\[
|A(j\omega)| = 1 \text{ at } \omega_T
\]

\[
\omega_T \approx \frac{g_{m1}}{C_C}
\]

\[
\omega_T \approx \frac{2\pi f_T}{C_C}
\]

\[
f_T \approx \frac{g_{m1}}{2\pi C_C}
\]
Slew rate

- \( I = C \frac{dV}{dt} \)
- Only limited current \( I_{\text{BIAS}} \) available to charge, discharge \( C_C \)
Slew rate

\[ I = C \frac{dV}{dt} \Rightarrow \frac{dV}{dt} = \frac{I_{BIAS}}{C_C} \]
Summary Op-amp:

- Stability
- Compensation
- Miller effect
- Phase Margin
- Unity gain frequency
- Slew Rate Limiting