Design example: common source amplifier with active load

Determine input DC bias and value of $R_b$ required for $V_{OUT}$ DC bias of 2.5V and DC drain current of 100$\mu$A

For $M_3$: Assume saturation, square law

\[
100\mu A = \frac{2.5E-6 \cdot 900}{2} \left( \frac{V_{GS3} + 1.5V}{2} \right)^2 [1 + (0.05V^2)(2.5V)]
\]

\[
V_{GS3} + 1.5V = \sqrt{\frac{100\mu A}{1.125}} \cdot \frac{2}{2.5E-6} \cdot \frac{900}{0.125} = \pm 0.890 V
\]

Choose $V_{DD} = 0.890 V$ for PMOS

\[
V_{GS} = -1.5V - 0.89V = -2.39V
\]

For $M_2$: Ignore channel length modulation

\[
I_B \approx I_D
\]

\[
R_b \text{ from Ohm's Law}
\]

\[
R_b = \frac{2.61V}{100\mu A} = 26.1 \text{ k}\Omega
\]

Disadvantage: $I_B$ sensitive to $V_{DD}$ variation

(Solution: bias block w/ bandgap $V$ ref)

---

Example process parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage $V_t$</td>
<td>+1.50</td>
<td>-1.50</td>
<td>V</td>
</tr>
<tr>
<td>Mobility- $C_{ox}$ product $\mu C_{ox}$</td>
<td>7.0 E-6</td>
<td>2.5 E-6</td>
<td>A/V²</td>
</tr>
<tr>
<td>Channel length modulation $\lambda$</td>
<td>0.03</td>
<td>0.05</td>
<td>V⁻¹</td>
</tr>
</tbody>
</table>
small signal gain

\[ g_m = \frac{2I_{D1}}{V_{GS1}V_{TH}} \]

\[ = \frac{2 \times 100 \text{mA}}{0.871} \]

\[ = 230 \text{ mA/V} \]

\[ r_{o1} = \frac{1}{\lambda_1 I_{D1}} \]

\[ = \frac{1}{(0.03)(100 \text{mA})} \]

\[ = 330 \text{ k}\Omega \]

\[ r_{o3} = \frac{1}{\lambda_3 I_{D3}} \]

\[ = \frac{1}{(0.05)(100 \text{mA})} \]

\[ = 200 \text{ k}\Omega \]

\[ \text{R}_{out} = \frac{1}{r_{o1}} + \frac{1}{r_{o3}} = \frac{1}{330 \text{ k}\Omega} + \frac{1}{200 \text{ k}\Omega} = 125 \text{ k}\Omega \]

\[ \frac{V_{out}}{V_{in}} = -g_m R_{out} = -\left(230 \text{ mA/V}\right)(125 \text{ k}\Omega) = -29 \]

\[ \text{Higher gain} \]

\[ \text{Smaller } V_{GS} - V_{TH} \]
CASCADE OF NONINTERACTING BLOCKS

\[
\frac{V_{out}}{V_{in}} = \left( \frac{V_{out}}{V_{2}} \right) \left( \frac{V_{2}}{V_{1}} \right) \left( \frac{V_{1}}{V_{in}} \right)
\]

PRODUCT OF INDIVIDUAL BLOCK TRANSFER FUNCTIONS!

\[
\frac{V_{M}}{V_{in}} = \frac{1}{1 + sRSC_m}
\]

\[\text{-founder of } R_1C \text{ at node } M\]

\[
\frac{V_{N}}{V_{1}} = \frac{1}{1 + sR_4C_N}
\]

\[\text{node } N\]

\[
A_2 \quad \frac{V_{out}}{V_{2}} = \frac{1}{1 + sR_2C_P}
\]

\[\text{output node}\]

\[\text{Figure 6.6 Cascade of amplifiers.}\]

\[
\frac{V_{out}}{V_{in}} = \frac{A_1 A_2}{(1 + sRSC_m)(1 + sR_4C_N)(1 + sR_2C_P)}
\]

\[\text{Each pole associated with one node}\]

\[f_{3dB} = \frac{1}{2\pi f_c}\]
EE4902 MILLER EFFECT.

Consider any amplifier (not necessarily an op-amp) with gain A, and some impedance Z from input to output: what impedance does it "look like"?

\[ i_x = \frac{V_x - AV_x}{Z} \]

\[ V_x = \frac{Z}{i_x (1-A)} \]

Impedance is reduced by factor \((1-A)\)

EXAMPLE: \(Z=10\Omega\) resistor
\(A = -9\); \(V_x = 1V\)

\[ I = \frac{V_x - (-9V)}{10\Omega} = 1A \]

Applying 1V causes 1A to flow: source "sees" a 1\(\Omega\) resistor! \(1\Omega = 10\Omega / (1-[-9])\)

**WHEN Z IS A CAPACITANCE:** \( Z = \frac{1}{j\omega C} \)

\[ \frac{V_x}{i_x} = \frac{1}{j\omega (1-A)C} \]

**APARENT VALUE OF C MULTIPLIED BY \(1-A\)!**

**LARGE INCREASE WHEN A IS INVERTING GAIN**
Figure 6.10
a common-source stage.

IF $C_{GS}$ DOMINATES

\[ V_{in} - \frac{1}{2\pi R_s C_{GS}} \]

IF $C_{DB}$ DOMINATES

\[ \frac{1}{2\pi R_o C_{DB}} \]

\[ C_{eq} = (1+g_m R_o) C_{gd} \]
ECE4902 Lecture 7

Common Source with Active Load
  Design Example
Current Mirror
  Diode connected MOSFET
  Resistor bias
Bandwidth (6.2)
  Gain-bandwidth product
Differential Pair

Hand In:
HW 3

Handouts:
Design Example
Transfer Function: Poles & Nodes
Miller Effect
3 Cases of Differential Pair
Bartlett's Bisection Theorem
Lab 7 Differential Pair Circuits
\[
\begin{align*}
I_{D1} &= 0 \quad I_{D2} = I_{SS} \\
V_{G1} &> V_{G2} \\
I_{D2} &> I_{D1} \\
I_{SS} &= 0
\end{align*}
\]

**Assume Drains V_{D1}, V_{D2} OK for Saturation**

\[
\begin{align*}
\frac{I_{SS}}{2} &\quad \frac{I_{SS}}{2} \\
V_{G1} &> V_{G2} \\
I_{D1} &> I_{D2} \\
I_{D1} &= I_{SS} \\
I_{D2} &= 0
\end{align*}
\]

**Connection:**

\[
V_{G1} = V_{G2} \\
\Rightarrow I_{D1} = I_{D2}
\]

**KCL at S Node:**

\[
I_{D1} + I_{D2} = I_{SS}
\]

---

**Currents:**

\[
\begin{align*}
I_{D1} &< I_{SS} \\
I_{D2} &< I_{SS}
\end{align*}
\]

\[
\begin{align*}
V_{O1} &< V_{D0} \\
V_{O2} &< V_{D0}
\end{align*}
\]

\[
\begin{align*}
V_{O1}, V_{O2} &< V_{O1}, V_{O2}
\end{align*}
\]

\[
\begin{align*}
V_{O1} &= \frac{I_{SS}R_0}{2} \\
V_{O2} &= \frac{I_{SS}R_0}{2}
\end{align*}
\]

\[
\begin{align*}
V_{D0} &= V_{O1} \\
V_{O1} &= V_{D0} - I_{SS}R_0
\end{align*}
\]

---

\[
\begin{align*}
V_{+} - V_{-} \\
V_{+} - V_{-}
\end{align*}
\]
KVL AROUND INPUT LOOP (GENERAL)

\[ V_+ - V_{GS1} + V_{GS2} = V_- \]

\[ V_+ - V_- = V_{GS1} - V_{GS2} \]

INPUT \underline{\Delta V_{GS}}

DIFFERENCE

\[ V_{GS1} > V_{GS2} \]

\[ V_{GS2} > V_{GS1} \]
DIFFERENTIAL OUTPUT VOLTAGE

WHAT IS SMALL SIGNAL GAIN? \(-g_m R_D\)

STEEPEST SLOPE, MOST LINEAR PART

ZERO \((V_+ - V_-)\) IN \(\rightarrow\) ZERO \((V_{01} - V_{02})\) OUT

SOFT, SYMMETRIC CLIPPING

\(+I_{SSR_D}\)
BARTLETT'S BISECTION THEOREM

Analysis using symmetry - "half circuit"

Consider two completely symmetrical circuits: a, b, c are connected points of symmetry

COMMON MODE

If \( V_1 = V_2 = V_c \) (both circuits have the same input; symmetric excitation) \( \Rightarrow \) then we can open all leads between points of symmetry without affecting circuit operation; no current flows across any connection.

EXAMPLE: \( i = 0 \) (no voltage drop across Rs due to symmetrical excitation. We can open this connection without affecting performance)

DIFFERENTIAL MODE

If \( V_1 = -V_2 \) (antisymmetric excitation) \( \Rightarrow \) then we can signal ground all leads between points of symmetry

EXAMPLE: by voltage divider, \( V_x = 0 \) regardless of \( V_d \). Therefore we can signal ground this connection without affecting circuit performance.
Any two signals can be expressed in terms of common mode, differential mode.

Consider any $V_1, V_2$:

$$V_c = \frac{V_1 + V_2}{2}$$

$$V_d = V_2 - V_1$$

Straightforward to verify that:

$$V_1 = V_c - \frac{V_d}{2}$$

$$V_2 = V_c + \frac{V_d}{2}$$

Key: analyze differential amplifier by decomposing inputs into $V_c$ and $V_d$, then using symmetry (Bartlett's bisection theorem) and superposition.
KVL TO OUTPUTS

\[ V_{01} = V_{DD} - I_{D1} R_D \]

\[ V_{02} = V_{DD} - I_{D2} R_D \]

DIFFERENTIAL HALF CIRCUIT

\[ \frac{V_{od}}{2} = -g_m R_D \frac{V_{id}}{2} \]

DIFFERENTIAL GAIN

\[ \frac{V_{od}}{V_{id}} = -g_m R_D \]