ECE4902 Lecture 2

Finish p-n junction
  Capacitance
  Built-in voltage
E Field word association
MOSFET symbols
MOSFET "building blocks"
MOSFET channel:
  Accumulation
  Depletion
  Inversion
MOSFET Fabrication steps
Carrier Motion: Mobility
IC Passives:
Resistor
  Sheet Resistance
  "Ω per square" concept
Capacitor

Handouts:
Lecture 2 Overview
MOSFET "building blocks"
MOSFET fabrication steps
MOS process parameters
Mobility figure
WHAT IS ELECTRIC FIELD ANYWAY?

\[ \mathbf{F} = q \mathbf{E} \]

LINES OF FORCE

E FIELD IS VECTOR MAGNITUDE & DIRECTION

RELATED TO CHARGE

TELLS YOU WHICH DIRECTION A + CHARGE WOULD GO (BECAUSE OF FORCE)

LINES KEEP TRACK OF CHARGE CONSERVATION

"RUBBER FORG BAND"

\[ \mathcal{E} = \frac{-dV}{dx} \]

VOLTAGE POTENTIAL CAN STORE ENERGY IN \( \mathcal{E} \) FIELD

\[ [\mathcal{E}] = \left[ \frac{V}{m} \right] \]
4 TERMINAL SYMBOL
SHOWS DIRECTION OF P-N JUNCTION
BODY → CHANNEL

\[ I_S = I_D \]

ARROW INDICATES POSITIVE CURRENT DIRECTION AT SOURCE

PMOS

DEVICES CONSTRUCTION OXIDE INSULATOR

DEVICE OXIDE INSULATOR

B "BODY" (SUBSTRATE)

P-N JCT B→D, B→S
ALWAYS KEEP THESE REVERSE BIASED

Figure 2.5 MOS symbols.

(a) No indication of S, D

(b) Usually digital on, off
MOSFET FUNCTIONS ("BUILDING BLOCKS")
GATE-SOURCE VOLTAGE CONTROLS DRAIN-SOURCE BEHAVIOR

**ANALOG SWITCH**

\[
\begin{align*}
V_{GS} & > V_{TH} : \text{ON} \\
V_{CTL} & \quad \text{ON/OFF}
\end{align*}
\]

\[
R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}
\]

**DIGITAL SWITCH**

\[
\begin{array}{c|c|c}
+SV & V_A & V_Y \\
- & +SV & 0V \\
- & 0V & +SV
\end{array}
\]

**"COMMON SOURCE" AMPLIFIER**

\[
\begin{align*}
V_{DD} & \quad I_{DR} \\
R & \quad -V_{OUT} \\
V_{IN} & \quad V_{GS}
\end{align*}
\]
BUFFER/LEVEL SHIFTER

\( V_{DD} \)

\( V_{IN} \)

\( V_{RS} \) (LARGE)

\( V_{GS} \)

\( V_{OUT} \)

\( R_L \) (SMALL)

"SOURCE FOLLOWER"

\( V_{DD} \)

\( V_{IN} \)

\( V_{OUT} \)

\( V_{GS} \)

\( t \)

CURRENT SOURCE

\( V_{BIAS} \)

\( V_{GS} \)

\( V_{DS} \)

\( I_D \)

RESISTOR (VOLTAGE CONTROLLED)

\( V_{CTL} \)

\( R_{on} \)

USED FOR ELECTRICAL CONTROL OF GAIN

CAPACITOR

\( V_C \)

THIN OXIDE

\( C = \frac{\varepsilon A}{d \cdot \tau_{ox}} \)

HIGH CAPACITANCE PER UNIT AREA
"Threshold Voltage"

\[ V_{GS} > V_{TH} \]

\[ I_D > 0 \]

\[ V_{DS} \]

Inversion

"Inverted" silicon at surface from p to n. Current \( I_D > 0 \) can flow if \( V_{DS} \) applied.

Depletion

\( V_{GS} > 0 \)

\[ I_D = 0 \]

\( E \) field from gate \( V_{GS} \) has depleted channel of mobile holes.

Depletion region \( S \rightarrow D \)

Fixed charge (dopant atoms) left behind.

\( V_{GS} = 0 \)

\[ I_D ? \]

OFF

S-D path: back-to-back diodes

\( I_D = 0 \)

Depletion region

\( V_{GS} < 0 \)

Accumulation

S-D channel even more p-type

\( I_D = 0 \)
a) 

\[ \text{SiO}_2 \] 

Not gate oxide use to define areas to be doped.

\[ p_{\text{substrate}} \]

b) 

"Ion implantation" 

N-type implant

\[ \text{\textquotedblright} n \text{ well}\text{\textquotedblright} \] 

\[ p_{\text{substrate}} \]

Defined with mask.

c) 

\[ n_{\text{well}} \] 

Strip away oxide.

PMOS devices will be in n well. "Local substrate".

\[ p_{\text{substrate}} \]

d) 

Channel stop implant

\[ \text{Si}_3\text{N}_4 \]

Regions where transistors are to be formed.

\[ p_{\text{substrate}} \]

Changes \( V_{TH} \) for unwanted parasitic MOSFETS.

e) 

Silicon that won't be MOSFETS

"Field" oxide

✓ Thick (insulator)

✓ Keep parasitics off.

\[ p_{\text{substrate}} \]
f) Threshold Adjust Implant
Threshold Adjust Implant
Gate Oxide

\[ t_{ox} \]

THIN

SO \[ V_{TH(n)} \approx -V_{TH(p)} \]
(GOOD FOR CMOS LOGIC)

---

g) Poly → Poly

\[ n^{\text{well}} \]

USE GATES AS MASKS FOR S, D DOPING
"SELF ALIGNED" PROCESS

---

h) NType Implant
NType Implant

\[ n^{+} \]

CONTACT THE \[ n^{\text{well}} \]
(SELF SUBSTRATE VOLTAGE OF PMOS)

---

i) PType Implant
PType Implant

\[ p^{+} \]

CONTACT SUBSTRATE

CHANNEL LENGTH
INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SCNA16_AMIS

TRANSISTOR PARAMETERS

<table>
<thead>
<tr>
<th>N/CHANNEL</th>
<th>P-CHANNEL</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum</td>
<td>Vth</td>
<td></td>
</tr>
<tr>
<td>Threshold</td>
<td></td>
<td></td>
</tr>
<tr>
<td>W/L</td>
<td>Vth</td>
<td>W, L</td>
</tr>
<tr>
<td>4.0/1.6</td>
<td>0.57</td>
<td>0.97</td>
</tr>
<tr>
<td>Idss</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20.0/1.6</td>
<td>183</td>
<td>-72 uA/um</td>
</tr>
<tr>
<td>Vth</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.55</td>
<td>-0.93</td>
<td></td>
</tr>
<tr>
<td>Vpt</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;PUNCH THROUGH&quot;</td>
<td>(10^{-6})</td>
<td></td>
</tr>
<tr>
<td>BREAK THRU OXIDE</td>
<td>(-10.0)</td>
<td></td>
</tr>
</tbody>
</table>

WIDE

<table>
<thead>
<tr>
<th>Ids0</th>
<th>&lt; 2.5</th>
<th>pA/um</th>
</tr>
</thead>
<tbody>
<tr>
<td>20.0/1.6</td>
<td>&lt; 2.5</td>
<td></td>
</tr>
</tbody>
</table>

LARGE

<table>
<thead>
<tr>
<th>Vth</th>
<th>0.58</th>
<th>-0.88</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vjbkd</td>
<td>16.6</td>
<td>-14.5</td>
</tr>
<tr>
<td>50/50</td>
<td>&lt;50.0</td>
<td>&lt;50.0</td>
</tr>
<tr>
<td>Ijlk</td>
<td>0.62</td>
<td>0.47</td>
</tr>
<tr>
<td>Gamma</td>
<td>(V^{0.5})</td>
<td></td>
</tr>
</tbody>
</table>

\(K' = (U_0 + Cox/2)\)

Low-field Mobility

\(35.7\)

\(632.73\)

\(212.68\) cm^2/V*s

\(\mu=\frac{e^{-}}{NHOMS}\) HOMS

\(\mu=\frac{e^{-}}{NHOMS}\) PMOS

Run for NMOS will be lower

Each wafer fabrication run has its own code; this run is designated "T6BF".

FEATURE SIZE is the minimum gate length; 1.6\(\mu\)m for this process.

TECHNOLOGY and RUN TYPE are more specific; these codes indicate added features in the process (for example, linear capacitors and BJTs).

\(V_{th}\) is the threshold voltage; MINIMUM refers to the smallest geometry devices allowed by the process design rules. For logic applications, often only minimum size devices are used.

\(I_{ds}\) is the current per unit width with maximum voltage (in the case of this process, 5V) applied for \(V_{GS}\). Expressing current this way allows the designer to rapidly determine required device size for a given current. For example, if 2mA of drive current is required for a P-channel MOSFET when the gate is fully turned on, the width should be

\(2\text{mA} / (86\mu\text{A}/\mu\text{m}) = 23.3\mu\text{m}\)

Note also that the threshold voltage \(V_{th}\) for the SHORT device is different than the MINIMUM case -- a second-order effect that SPICE needs to keep track of.

Vpt is the punch-through voltage, beyond which the device will be damaged.

This is the leakage current per unit width when \(V_{GS}=0\). An important parameter for analog switch design, especially in sample-and-hold circuits when the hold capacitor can be partially discharged by the leakage current of a MOSFET which should be "off".

Again, note that the threshold voltage is affected by device geometry.

\(V_{jgbk}\) is the breakdown voltage of the active-substrate pn junction;

\(I_{ljk}\) is the reverse bias leakage current of the junction.

\(Gamma\) is the body-effect parameter, which expresses how the threshold voltage is affected by the source-substrate reverse bias voltage.

\(K'\) is the transconductance parameter used in some expressions of the square law

\[I_D = \frac{\mu C_{OX} W}{2 L} (V_{GS} - V_{TH})^2\]

Low-field mobility is the value of \(\mu\) for E fields below the velocity saturation limited region.
**Sheet resistance:** These are the numbers to use when determining the physical dimensions of a resistor to achieve a certain value of resistance. The layers are:

- **N+** Heavily doped region of N-type diffusion used for source, drain of N-channel MOSFETs
- **P+** Heavily doped region of P-type diffusion used for source, drain of P-channel MOSFETs
- **POLY** Polysilicon metal used for gates of MOSFETs
- **POLY2** A second layer of polysilicon which can also be used for MOSFET gates (Also, POLY and POLY2 can be used with thin oxide between to make a linear capacitor (See capacitance parameters below)
- **PBASE** A moderately doped region of P-type diffusion used as the base for NPN bipolar transistors
- **M1** First layer of aluminum metalization; much lower sheet resistance than polysilicon or diffusion
- **M2** Second layer of metalization; lowest sheet resistance since thickness of M2 is greater than thickness of M1
- **N_W** Lightly doped region of N-type diffusion used as a well (sort of a "local substrate") used for P-channel MOSFETs

**Gate Oxide Thickness:** This is the oxide thickness tox used to determine the gate capacitance per unit area. Check by comparing to the gate oxide capacitance per unit area:

\[
\frac{t_{ox}}{t_{ox}^{M1}} = \frac{3.9(8.85E-12 F/m)}{306E-10 m} = 1.13E-3 F/m^2
\]

Which agrees pretty well with the 1128aF/um^2 for POLY-to-N+ shown below.

**CAPACITANCE PARAMETERS**

<table>
<thead>
<tr>
<th></th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>N_W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>291</td>
<td>302</td>
<td>36</td>
<td>37</td>
<td>21</td>
<td>13</td>
<td>129</td>
</tr>
<tr>
<td>Area (N+active)</td>
<td>1128</td>
<td>730</td>
<td>50</td>
<td>26</td>
<td>46</td>
<td>23</td>
<td></td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>1110</td>
<td>723</td>
<td>46</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area (poly)</td>
<td>592</td>
<td>46</td>
<td>46</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area (poly2)</td>
<td>46</td>
<td></td>
<td>46</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area (metall)</td>
<td>38</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>79</td>
<td>160</td>
<td>31</td>
<td>27</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>58</td>
<td>44</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fringe (metall)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overlap (N+active)</td>
<td>173</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>231</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

These are parallel-plate capacitance (per unit area) between the layers indicated. For example, a capacitor using M1 and M2 as the plates will have a capacitance of 38aF/um^2 (also is 1E-18) per micron squared. A capacitor 100um x 100um has an area of 1E+4um^2, so the capacitance would be 380E-15 F, or 0.38pF.

Fringe and overlap capacitances are edge effects, and therefore are given per unit length. The 100um x 100um capacitor mentioned in the example above would have a perimeter of 400um. The fringe capacitance from M1 to M2 is 55aF/um. Thus the capacitance due to the fringing field would be (400um)(55aF/um)=22 E-15 F = 22fF. Total for the 100um x 100um capacitor will be the sum of contributions from parallel plate + fringing: 0.38pF + 22fF = 0.402pF.