**PURPOSE:**

The purpose of this lab is to measure the performance of an op-amp designed from individual MOSFETs. This op-amp, shown in Fig. 8-1, combines all of the major circuit techniques we have been developing this term:

- Differential pair M1-M2 (input stage)
- Common source amplifier M5 (output stage)
- Current source with "bias rail" M6, M7, M8 (bias for differential pair and output stage)
- Current mirror load M3-M4 (for input stage high gain and single-ended to differential conversion)
- Active load M8 (for common source stage)
- Compensation using \( C_{\text{COMP}} \) and the Miller effect (for stability)

**NOTE:** Be sure to record ALL results in your laboratory notebook.

**NOTE:** This lab involves construction and measurement of circuits with very high gains. It is extremely important to use bypass capacitors \( C_{\text{BP1}} \) and \( C_{\text{BP2}} \) on the supply rail(s) to keep the power supply voltages clean. Also, keep wire leads as short as possible to prevent noise coupling into the circuit.

**NOTE: DO NOT DISASSEMBLE THIS CIRCUIT AT THE END OF THE LAB! YOU WILL USE THIS CIRCUIT (ADDING \( C_{\text{COMP}} \)) IN THE NEXT LAB!**
Figure 8-1.

C_{BP1} \approx 0.01 \mu F

C_{BP2} \approx 0.01 \mu F

V_{DD} = +5V

V_{SS} = -5V

R_b = 150k\Omega

M_1, M_2, M_3, M_4, M_5, M_6, M_7, M_8

V_{G3}, V_{G5}, V_{G6}, V_{S1}

V_{-}, V_{+}, V_{out}

All P: \frac{900}{10}

All N: \frac{350}{10}
CIRCUIT: CMOS OP-AMP

L8-1. Construct the circuit shown in Figure 8-1. (Note that this circuit requires three (3) MC14007 chips). **Don't install C_{COMP} until later, in the next lab.** Double check your wiring - with so many connections, it's easy to make wiring errors. R_{B} is chosen for a DC bias current of about 50µA in M7 (bias for input differential pair) and M8 (active load for output common source stage).

FUNCTIONALITY / DC BIAS LEVEL

L8-2. To check the op-amp for functionality, connect as shown in Figure 8-2 to check open loop performance. To make the (very small) input voltage for the op-amp, use the 1kΩ/10Ω attenuator network shown. The function generator output should be around 1V peak; this will give a voltage of about 10mV peak into the op-amp input.

The op-amp output should be a rail-to-rail square wave, due to the high open-loop gain of the op-amp. Adjust the amplitude and offset of the function generator until the op-amp output is not clipped. Measure the open-loop gain of the op-amp. Be sure to use a low enough frequency (~100Hz or even lower) so that the output is a clean triangle wave (not rounded due to bandwidth limitation). Remember to account for the attenuation of the 1kΩ/10Ω network!

Use the multiple-channel capability of your scope to “follow” the signal along the path from input to output. Using a separate scope channel for each, look at the signal at the input (V_{in}), first stage output (V_{G5}), and output V_{out}. Note the polarity, amplitude, and DC bias level at each point.

L8-3. Indirectly measure the DC bias level by measuring the voltage drop across R_{B}. Calculate the resulting bias current; anything close to 50µA is OK. Be sure to record the exact value; you will need it later when calculating transconductances and the expected slew rate.
Lab Writeup

As mentioned in Lab 1, the purpose of these labs is to help "close the loop" in your understanding of the complete integrated circuit design process. We can approach this op-amp circuit at three different levels: hand analysis, simulation, and the measurements of actual circuits. Your writeup should describe the measured performance relative to a hand analysis of the circuit. For the open-loop op-amp (comparator):

W8-1. Measurement:

Report the measured DC bias current from L8-3 and the measured small-signal open-loop gain from L8-2.

W8-2. Hand Analysis:

From the measured DC bias current and the parameters you extracted for your MOSFETs (including the channel length modulation parameter \( \lambda \)), determine:
The transconductances \( g_{m1} \) and \( g_{m5} \) of M1 and M5.
The small-signal output resistances \( r_{ds2}, r_{ds4}, r_{ds5}, r_{ds8} \), for M2, M4, M5, M8.
Draw the small-signal model of the amplifier as a cascade of two general amplifier stage (\( r_{in}/G_{m}/r_{out} \)) models.
Determine the expected small-signal open-loop gain, and compare to your measured value from L8-2

W8-3. Simulation

Perform a DC sweep to get the input-output characteristic. Be sure to use enough points on the sweep to avoid aliasing effects. Consider a sweep of \( V_{IN} \) from -50mV to +50mV with a step size of 0.1mV. Use the AB markers to get the slope (small signal gain) near the center of the linear region. Compare with your measured and calculated results.

Does the input-output characteristic pass exactly through the origin? (Hint: no!) Note this "systematic offset" which we’ll look at in more detail in a future lecture.