

Xilinx Device Families

Family / Dev. Board	Device	Slices ⁵	I/O Pins/Pads	Digital Clock Managers	Distributed RAM (Kbits)	Block RAM (Kbits)	18x18 Mult. / XtremeDSP ¹	RocketIO Transceivers	IBM PPC 405 Cores ²	Approx. MicroBlaze ³
Spartan-3 (Low-Cost)	<i>(all)</i>	768 - 33,280	124 - 784	2 - 4	12 - 520	72 - 1,872	4 - 104	0	0	1 - 71
Digilent S3	XC3S200	1,920	173	4	30	216	12	0	0	4
Virtex-II	<i>(all)</i>	256 - 46,592	88 - 1,108	4 - 12	8 - 1,456	72 - 3,024	4 - 168	0	0	0 - 110
Memex V2MB	XC2V1000 ⁴	5,120	432	8	160	720	40	0	0	12
Virtex-II Pro	<i>(all)</i>	1,408 - 44,096	204 - 1,164	4 - 12	44 - 1,378	216 - 7,992	12 - 444	4 - 20	0 - 2	3 - 104
Xilinx ML310	XC2VP30	13,696	644	8	428	2,448	136	8	2	32
Virtex-4 LX (Logic)	<i>(all)</i>	6,144 - 89,088	320 - 960	4 - 12	96 - 1,392	864 - 6,048	32 - 96	0	0	12 - 185
Xilinx ML401	XC4VLX25	10,752	448	8	168	1,296	48	0	0	22
Virtex-4 SX (DSP)	<i>(all)</i>	10,240 - 24,576	320 - 640	4 - 8	160 - 384	2,304 - 5,760	128 - 512	0	0	21 - 51
Xilinx ML402	XC4VSX25	10,240	320	4	160	2,304	128	0	0	21
Virtex-4 FX (MCU)	<i>(all)</i>	5,472 - 63,168	320 - 896	4 - 20	86 - 987	648 - 9,936	32 - 192	0 - 24	1 - 2	11 - 131
Xilinx ML403	XC4VFX12	5,472	320	4	86	648	32	0	1	11

¹ In Virtex-4 devices, XtremeDSP Slices include an 18x18 multiplier, an adder, and a 48-bit accumulator; in all other devices XtremeDSP slices are not available and this number refers to the number of dedicated 18x18 Multipliers available.

² Virtex-4 FX devices feature 2 dedicated Ethernet 10/100/1000 MACs per PPC core.

³ Actual maximum number of MicroBlaze soft processors will be lower due to routing issues. PicoBlaze processors are approx. 4-5 times smaller than MicroBlaze.

⁴ This device is also featured on the existing PPL digital boards.

⁵ A "logic cell" is a measurement of device capacity defined by Xilinx as a 4-input LUT and a connected register. On these device families, one Slice is equal to 2.25 Logic Cells, and each Configurable Logic Block (CLB) contains 4 (only slightly different) slices.

Processor Performance

	PicoBlaze		MicroBlaze		PPC 405	
	MHz	MIPS	MHz	DMIPS *	MHz	DMIPS *
Spartan-3	88	44	80	64	N/A	
Virtex-II	152	76	125	100	N/A	
Virtex-II Pro	200	100	150	120	400	600
Virtex-4	200	100	150	120	450	700

* DMIPS = Dhrystone MIPS (more accurate MIPS measurement)

MicroBlaze logic requirements

	Logic Cells	~ Slices *
Spartan-3	1050	467
Virtex-II	950	423
Virtex-II Pro	950	423
Virtex-4	1080	480

PicoBlaze requires ~96 slices

* On these device families, one slice is equal to 2.25 logic cells.

Original Xilinx Device Tables

Table 1: Summary of Spartan-3 FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)			Distributed RAM (bits ¹)	Block RAM (bits ¹)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50 ²	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200 ²	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400 ²	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000 ^{2,3}	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500 ³	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000 ³	4M	62,208	96	72	6,912	432K	1,728K	96	4	712	312
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	784	344

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.
2. These devices are available in Xilinx Automotive versions as described in [DS314](#): Spartan-3 Automotive XA FPGA Family.
3. XC3S1000, XC3S1500, and XC3S4000 are also available in lower static power versions as described in [DS313](#): Spartan-3L Low Power FPGA Family.

Table 1: Virtex-II Field-Programmable Gate Array Family Members

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads ⁽¹⁾
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

Notes:

1. See details in [Table 2](#), "Maximum Number of User I/O Pads".

Table 1: Virtex-II Pro / Virtex-II Pro X FPGA Family Members

Device ⁽¹⁾	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells ⁽²⁾	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8 ⁽⁴⁾	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0 ⁽³⁾ , 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0 ⁽³⁾ or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20 ⁽⁴⁾	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0 ⁽³⁾ or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:

1. -7 speed grade devices are not available in Industrial grade.
2. Logic Cell \approx (1) 4-input LUT + (1)FF + Carry Logic
3. These devices can be ordered in a configuration without RocketIO transceivers. See Table 3 for package configurations.
4. Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

Table 1: Virtex-4 FPGA Family Members

Device	Configurable Logic Blocks (CLBs) ⁽¹⁾				XtremeDSP Slices ⁽²⁾	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transceiver Blocks	Total I/O Banks	Max User I/O
	Array Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VLX15	64 x 24	13,824	6,144	96	32	48	864	4	0	N/A	N/A	N/A	9	320
XC4VLX25	96 x 28	24,192	10,752	168	48	72	1,296	8	4	N/A	N/A	N/A	11	448
XC4VLX40	128 x 36	41,472	18,432	288	64	96	1,728	8	4	N/A	N/A	N/A	13	640
XC4VLX60	128 x 52	59,904	26,624	416	64	160	2,880	8	4	N/A	N/A	N/A	13	640
XC4VLX80	160 x 56	80,640	35,840	560	80	200	3,600	12	8	N/A	N/A	N/A	15	768
XC4VLX100	192 x 64	110,592	49,152	768	96	240	4,320	12	8	N/A	N/A	N/A	17	960
XC4VLX160	192 x 88	152,064	67,584	1056	96	288	5,184	12	8	N/A	N/A	N/A	17	960
XC4VLX200	192 x 116	200,448	89,088	1392	96	336	6,048	12	8	N/A	N/A	N/A	17	960

Table 1: Virtex-4 FPGA Family Members (Continued)

Device	Configurable Logic Blocks (CLBs) ⁽¹⁾				XtremeDSP Slices ⁽²⁾	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transceiver Blocks	Total I/O Banks	Max User I/O
	Array Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VSX25	64 x 40	23,040	10,240	160	128	128	2,304	4	0	N/A	N/A	N/A	9	320
XC4VSX35	96 x 40	34,560	15,360	240	192	192	3,456	8	4	N/A	N/A	N/A	11	448
XC4VSX55	128 x 48	55,296	24,576	384	512	320	5,760	8	4	N/A	N/A	N/A	13	640
XC4VFX12	64 x 24	12,312	5,472	86	32	36	648	4	0	1	2	N/A	9	320
XC4VFX20	64 x 36	19,224	8,544	134	32	68	1,224	4	0	1	2	8	9	320
XC4VFX40	96 x 44	41,904	15,552	243	48	144	2,592	8	4	2	4	12	11	448
XC4VFX60	128 x 52	56,880	25,280	395	128	232	4,176	12	8	2	4	16	13	576
XC4VFX100	160 x 68	94,896	42,176	659	160	376	6,768	12	8	2	4	20	15	768
XC4VFX140	192 x 84	142,128	63,168	987	192	552	9,936	20	8	2	4	24	17	896

Notes:

- One CLB = Four Slices = Maximum of 64 bits.
- Each XtremeDSP slice contains one 18 x 18 multiplier, an adder, and an accumulator