R. Ludwig and G. Bogdanov
"RF Circuit Design: Theory and Applications"
2nd edition

Figures for Chapter 7

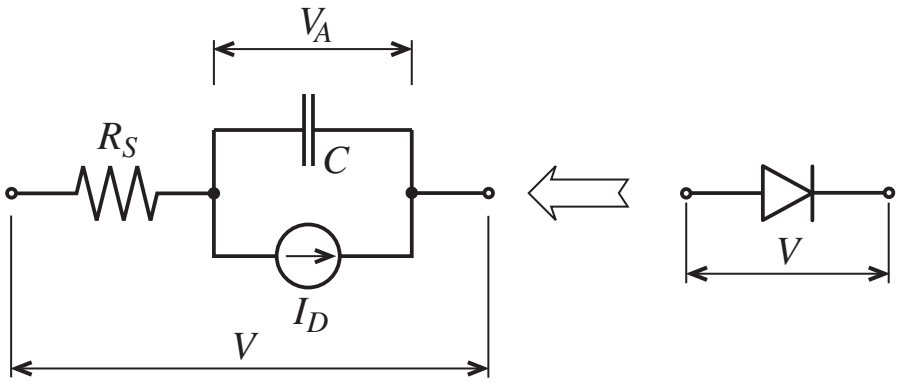
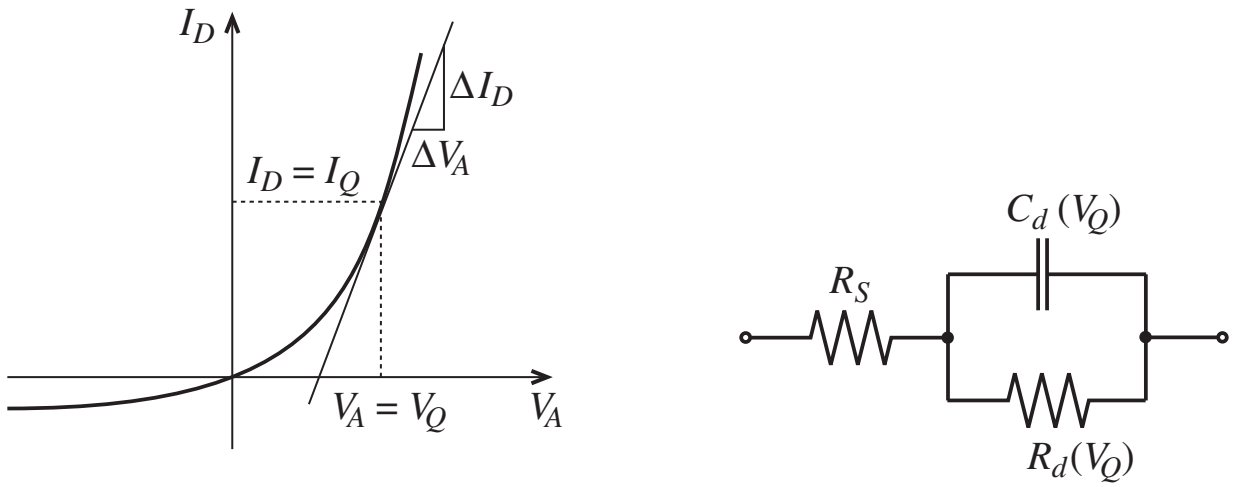


Figure 7-1 Large-scale diode model.

Table 7-1 Diode model parameters and their corresponding SPICE parameters

Symbol	SPICE	Description	Typical values
I_S	IS	saturation current	1 fA–10 μA
n	N	emission coefficient	1
τ_T	TT	transit time	5 ps–500 μs
R_S	RS	ohmic resistance	0.1–20 Ω
V_{diff}	VJ	barrier voltage	0.6–0.8 V (*pn*) 0.5–0.6 V (Schottky)
C_{J0}	CJ0	zero-bias junction capacitance	5–50 pF (*pn*) 0.2–5 pF (Schottky)
m	M	grading coefficient	0.2–0.5
W_g	EG	bandgap energy	1.11 eV (Si) 0.69 eV (Si-Schottky)
p_t	XTI	saturation current temperature coefficient	3 (*pn*) 2 (Schottky)



(a) tangent approximation at Q-point

(b) linear circuit model

Figure 7-2 Small-signal forward biased diode model.

Table 7-2 Diode model parameters for different temperatures

T, K	250	300	350	400
$W_g(T)$, eV	1.128	1.115	1.101	1.086
$I_s(T)$, A	5.1×10^{-19}	5.0×10^{-15}	3.3×10^{-12}	3.8×10^{-10}
V_Q, V	0.979	0.898	0.821	0.748
R_d, Ω	0.5	0.6	0.7	0.8
C_d, pF	999.5	832.9	713.9	624.7

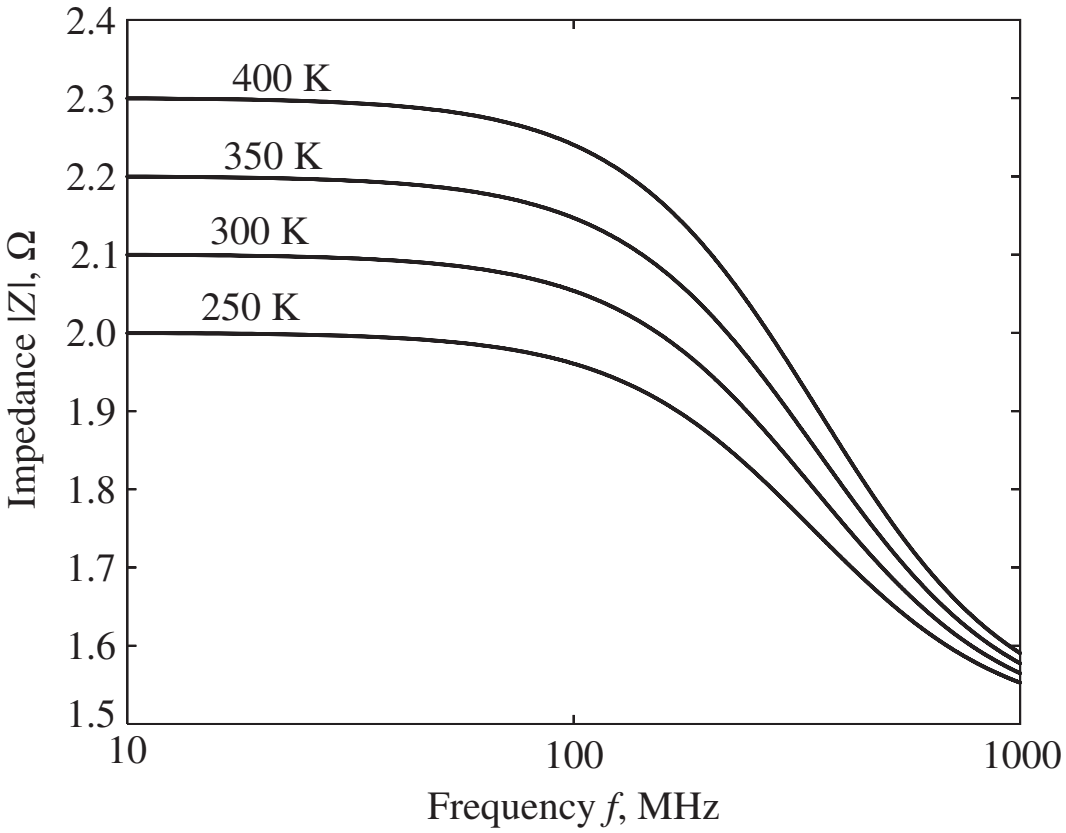
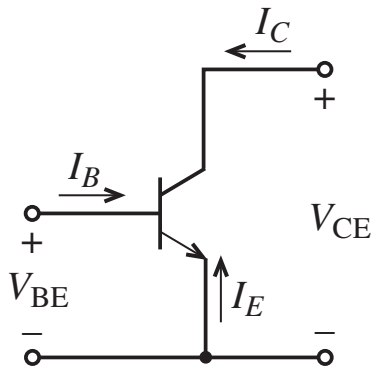
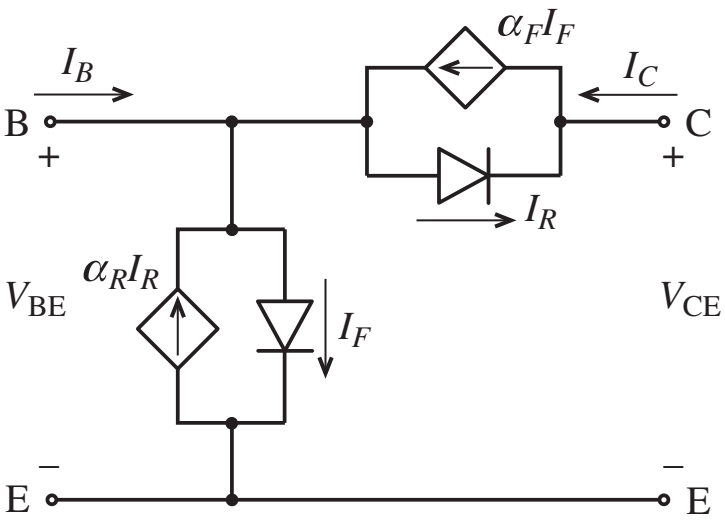


Figure 7-3 Frequency behavior of the diode impedance for different junction temperatures.



(a) Voltage and current convention for *npn* transistor



(b) Ebers-Moll circuit model

Figure 7-4 Large-signal Ebers-Moll circuit model.

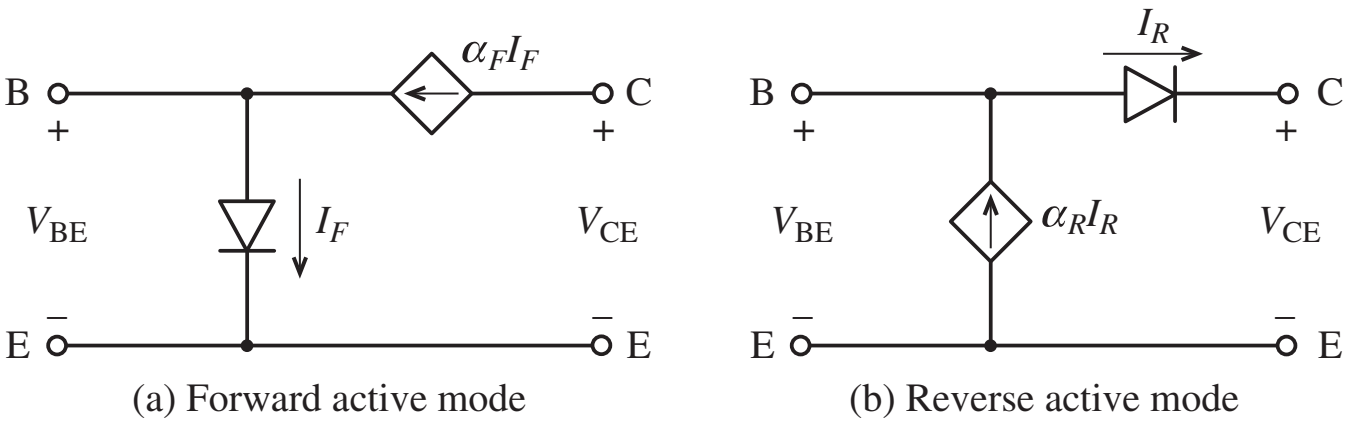
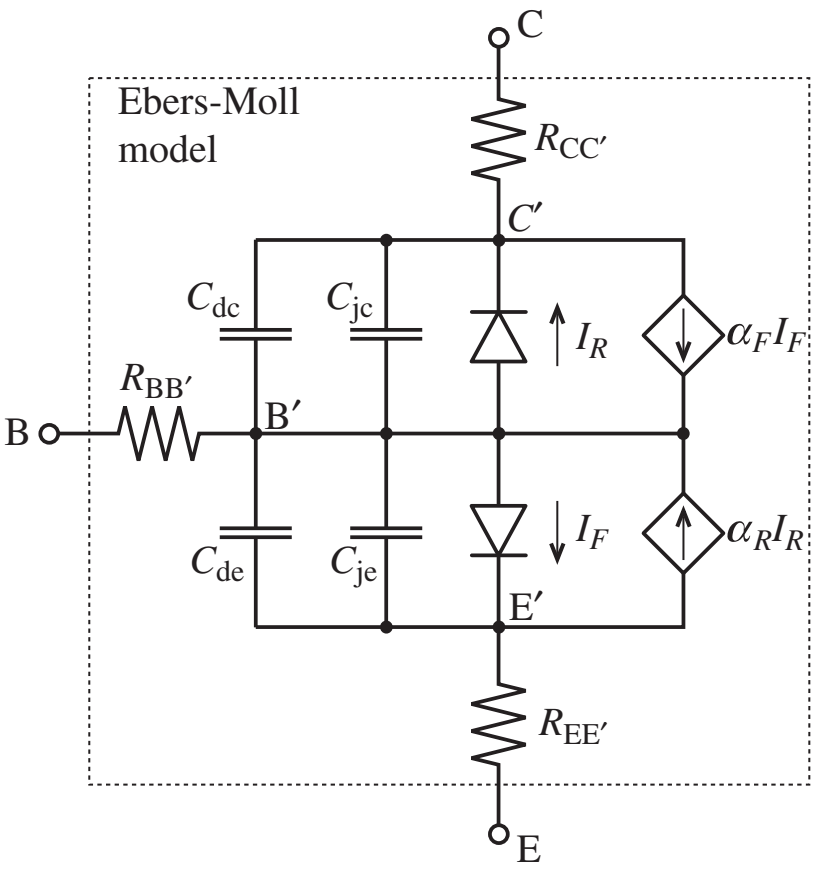
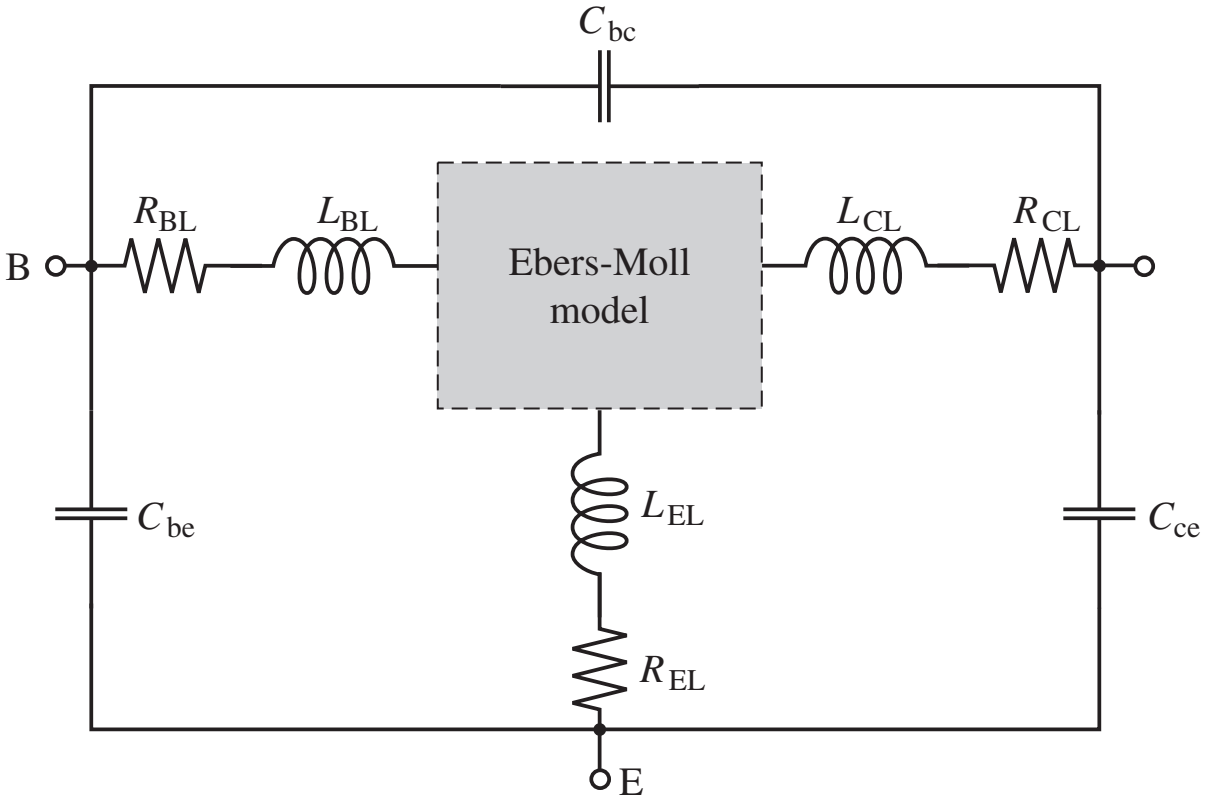


Figure 7-5 Simplified Ebers-Moll equations for forward and reverse active modes.



(a) Dynamic Ebers-Moll chip model



(b) RF model with parasitic terminal effects

Figure 7-6 Dynamic Ebers-Moll model and parasitic element refinements.

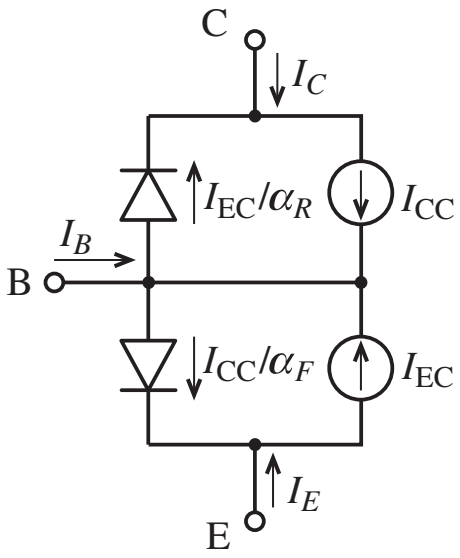


Figure 7-7 Transport representation of static Ebers-Moll model.

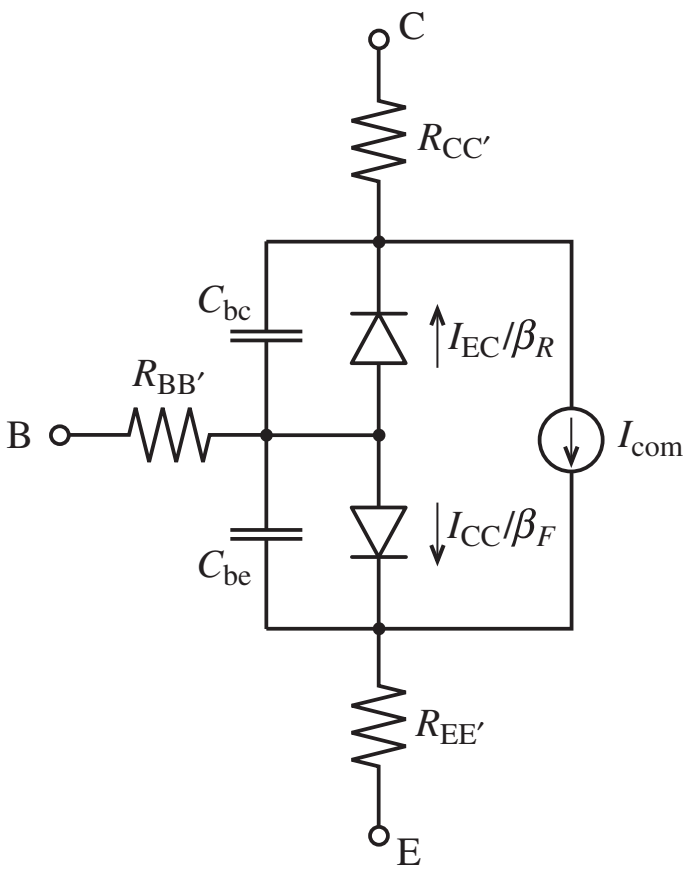


Figure 7-8 Dynamic Ebers-Moll transport model with single current source.

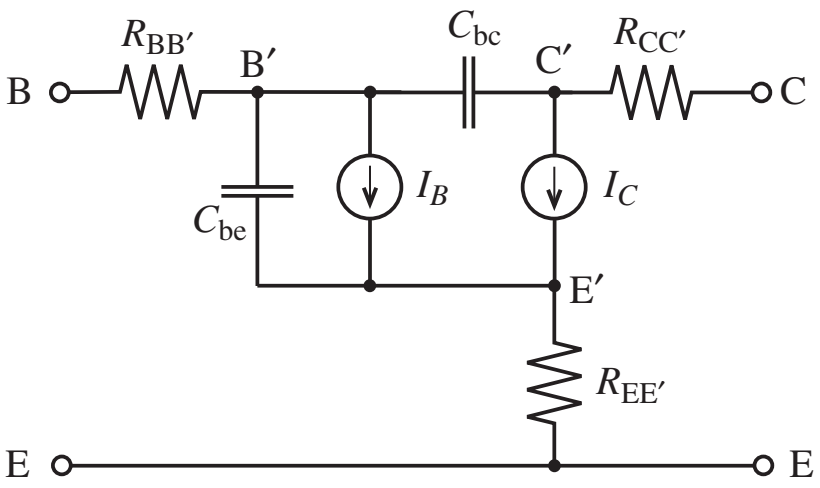


Figure 7-9 Large-signal BJT model in forward active mode.

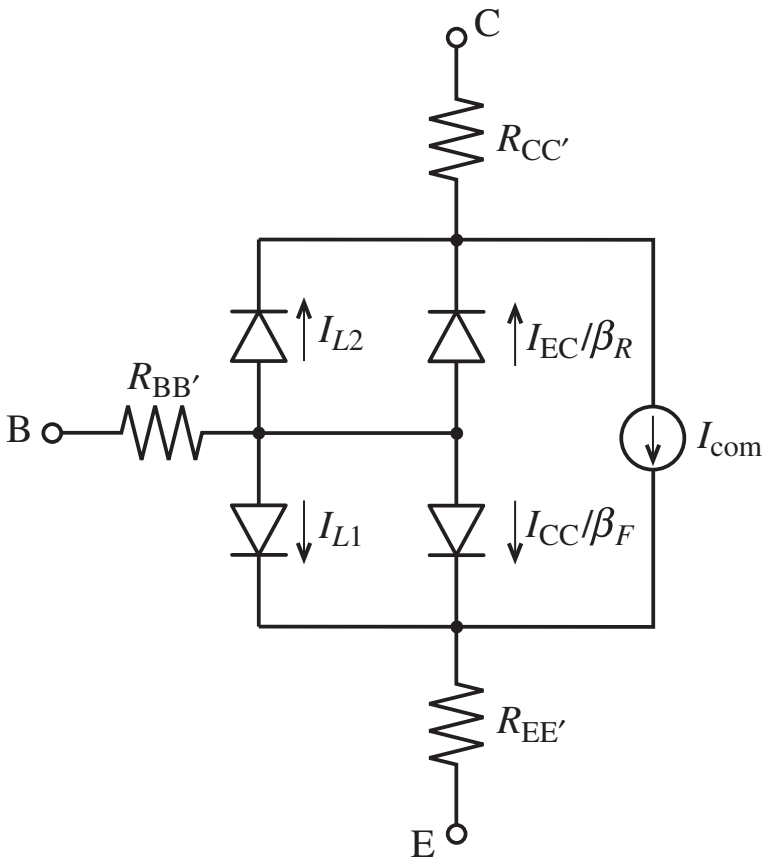


Figure 7-10 Static Gummel-Poon model.

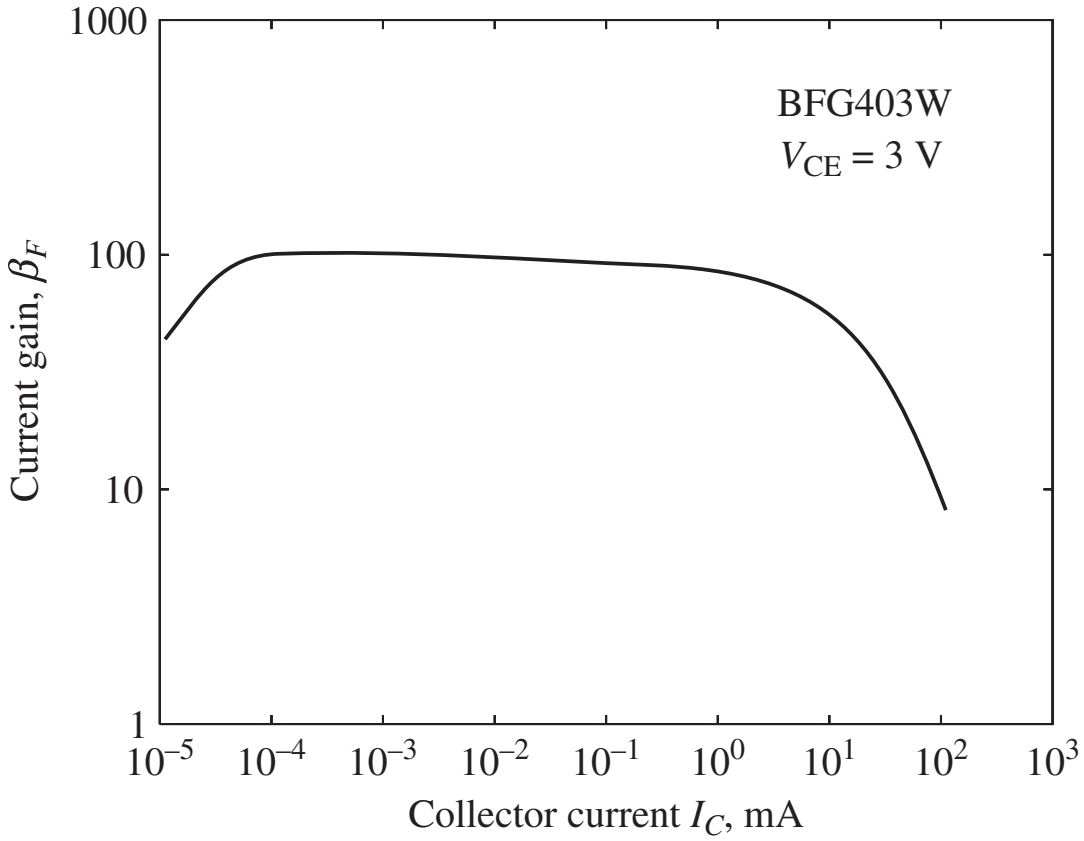


Figure 7-11 Typical dependence of β_F on the collector current I_C for a fixed collector-emitter voltage V_{CE}.

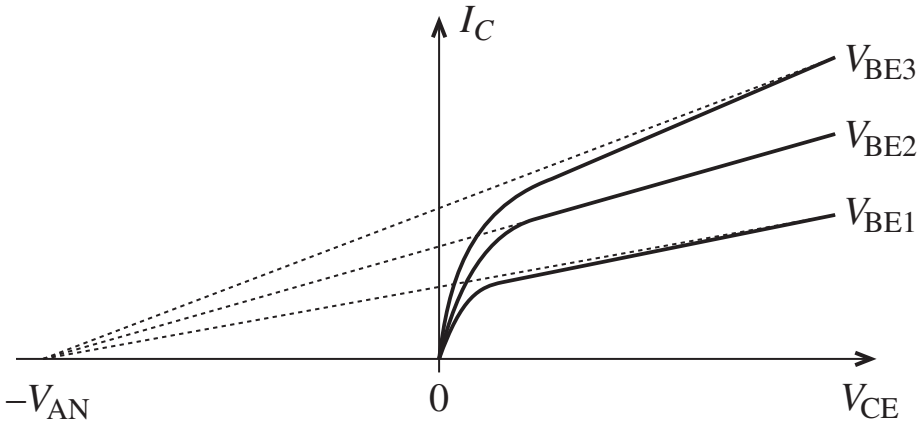


Figure 7-12 Collector current dependence on V_{CE} and its approximation through the Early voltage V_{AN}.

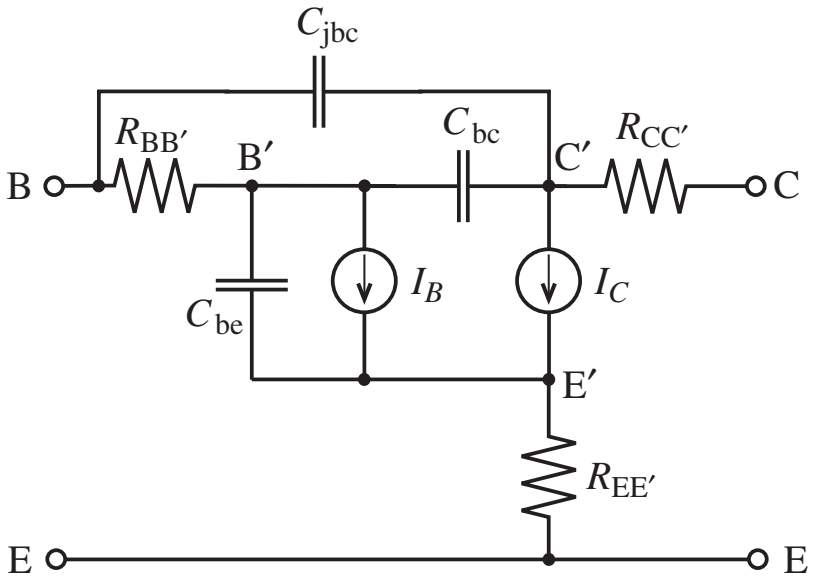


Figure 7-13 Large-signal Gummel-Poon model in forward active mode.

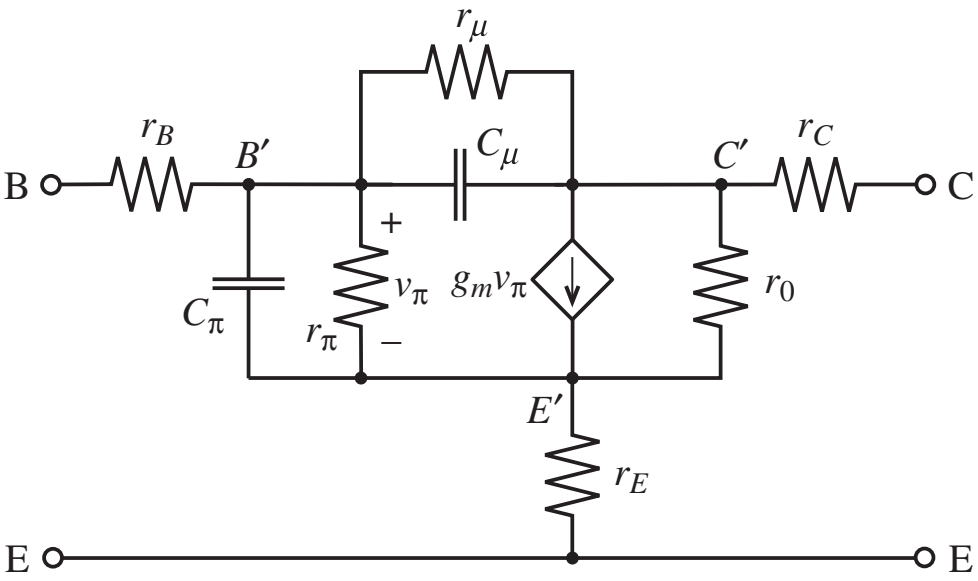


Figure 7-14 Small-signal hybrid-π Ebers-Moll BJT model.

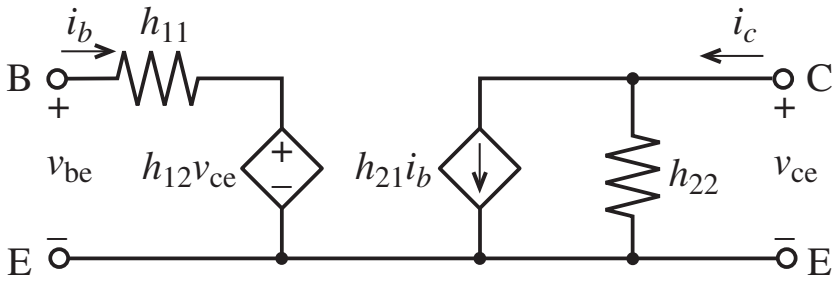
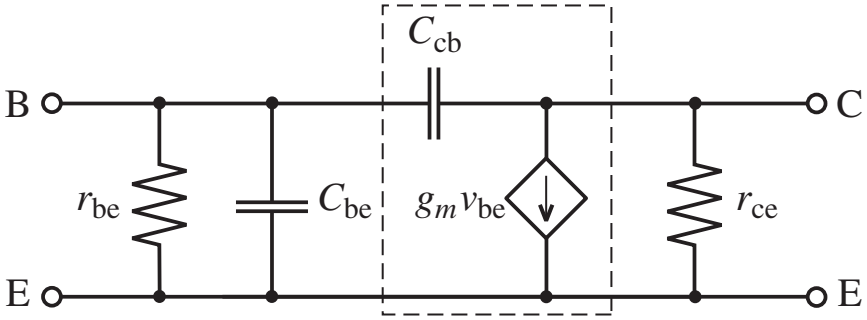
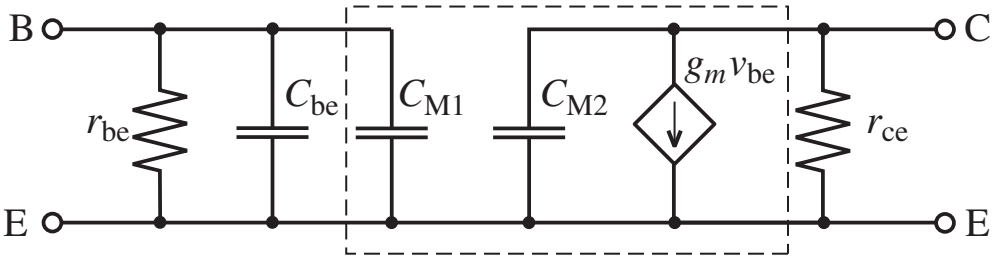


Figure 7-15 Generic *h*-parameter BJT representation with two sources.

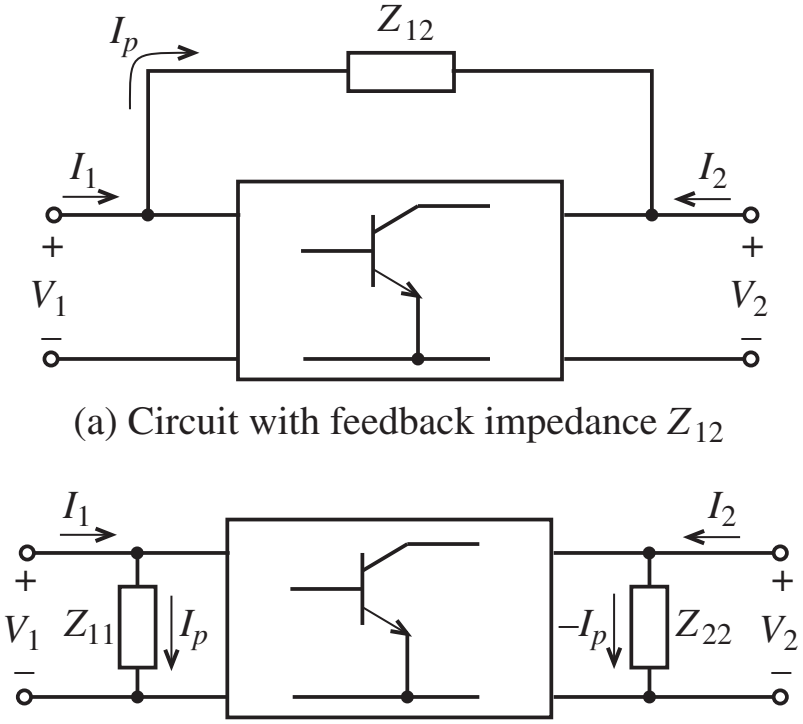


(a) RF circuit model



(b) Equivalent circuit model

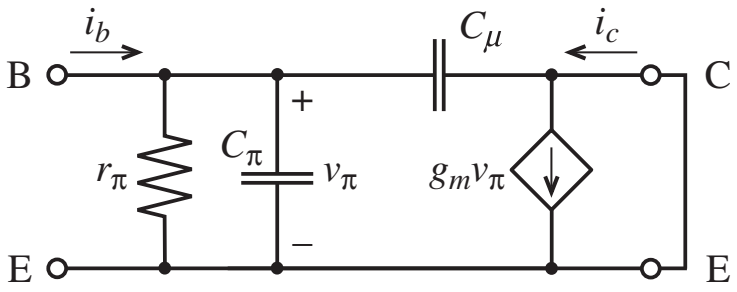
Figure 7-16 RF small-signal circuit model and converted circuit model using the Miller effect.



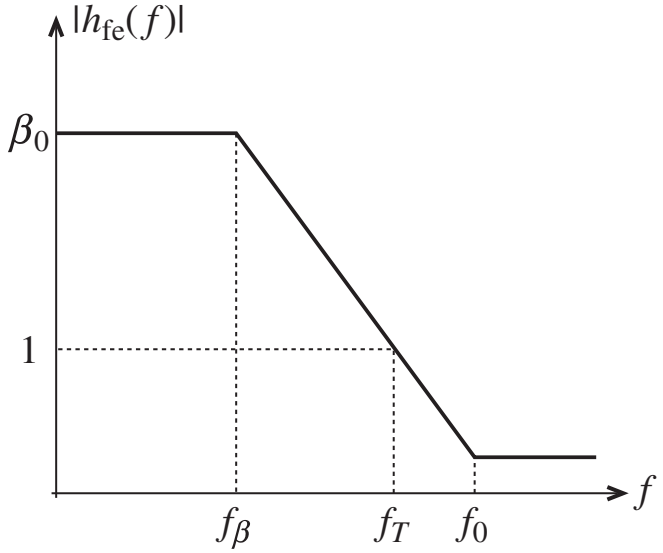
(a) Circuit with feedback impedance Z_{12}

(b) Equivalent form

Figure 7-17 Miller transformation of feedback impedance.



(a) Short-circuited hybrid-π model



(b) Amplification versus frequency behavior on a log-log scale

Figure 7-18 Short-circuit current gain of BJT model.

Table 7-3 SPICE parameters of the BJT

Symbol	Description	Typical value
β_F	forward current gain	145
I_S	saturation current	5.5 fA
V_{AN}	forward Early voltage	30 V
τ_F	forward transit time	4 ps
C_{JC0}	base-collector junction capacitance at zero applied junction voltage	16 fF
C_{JE0}	base-emitter junction capacitance at zero applied junction voltage	37 fF
m_C	collector capacitance grading coefficient	0.2
m_E	emitter capacitance grading coefficient	0.35
$V_{\mathrm{diff}_{\mathrm{BE}}}$	base-emitter diffusion potential	0.9 V
$V_{\mathrm{diff}_{\mathrm{BC}}}$	base-collector diffusion potential	0.6 V
r_B	base body resistance	125 Ω
r_C	collector body resistance	15 Ω
r_E	emitter body resistance	1.5 Ω
L_B	base lead inductance	1.1 nH
L_C	collector lead inductance	1.1 nH
L_E	emitter lead inductance	0.5 nH

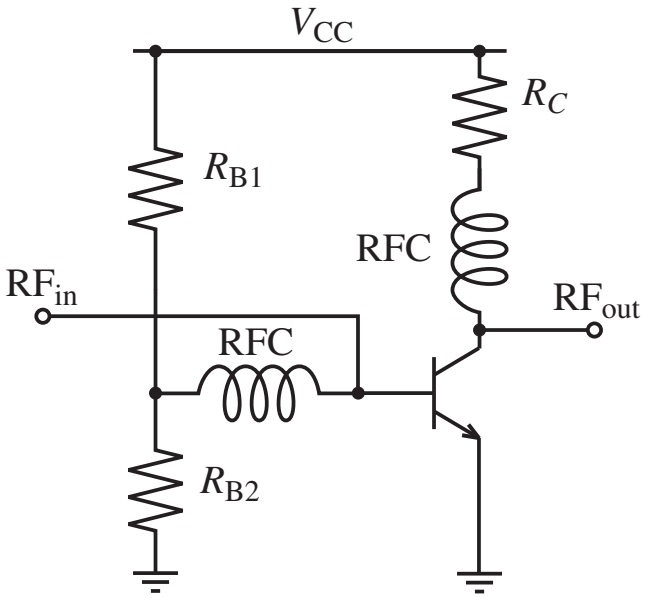


Figure 7-19 Biasing a BJT in common-emitter configuration.

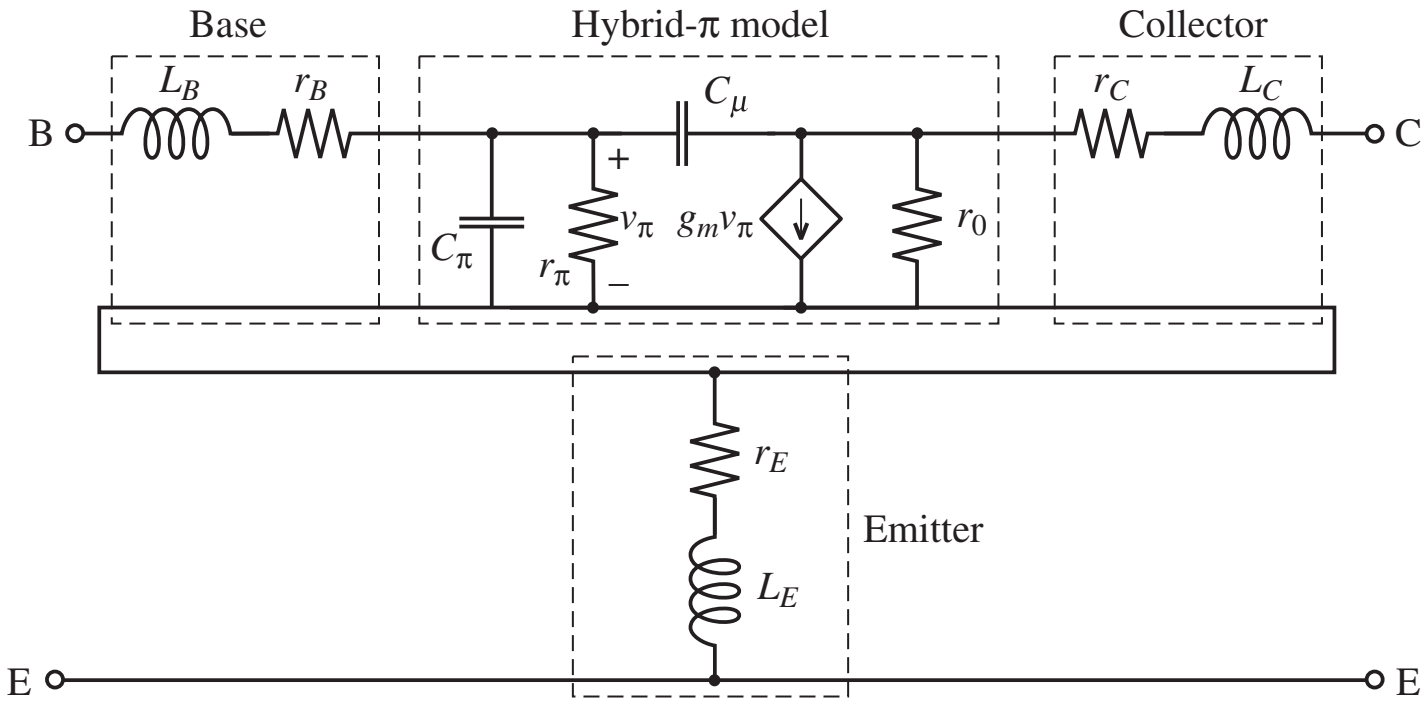
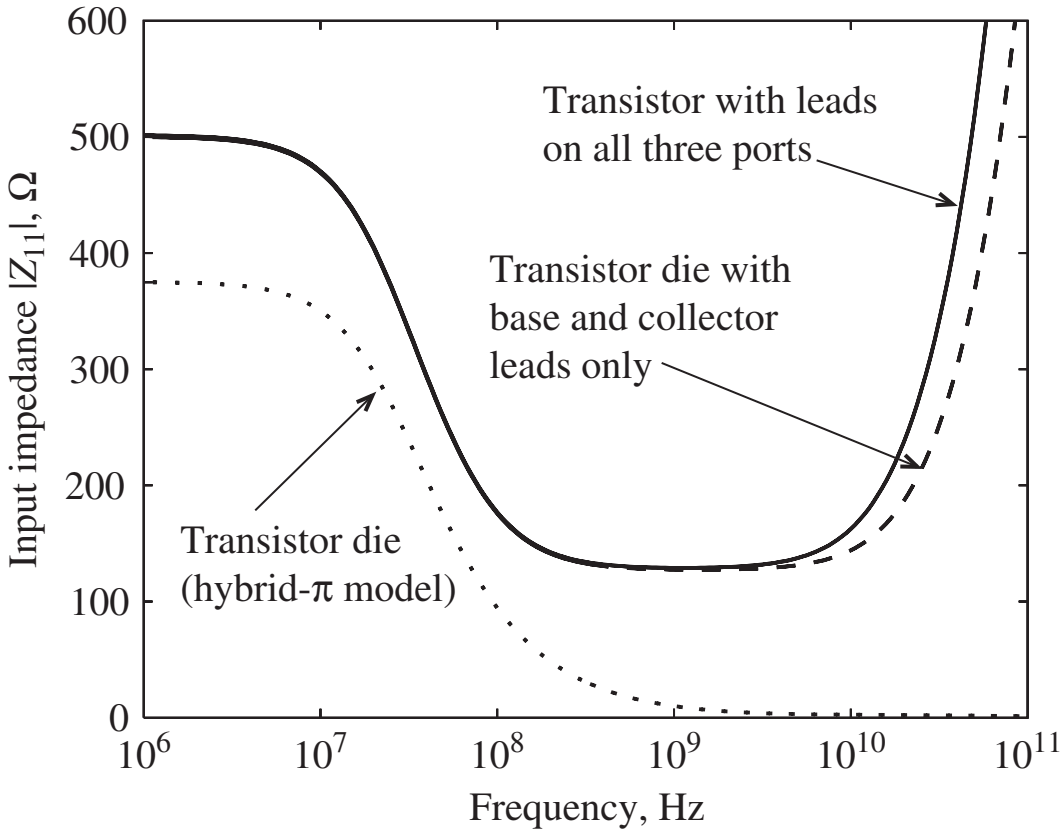
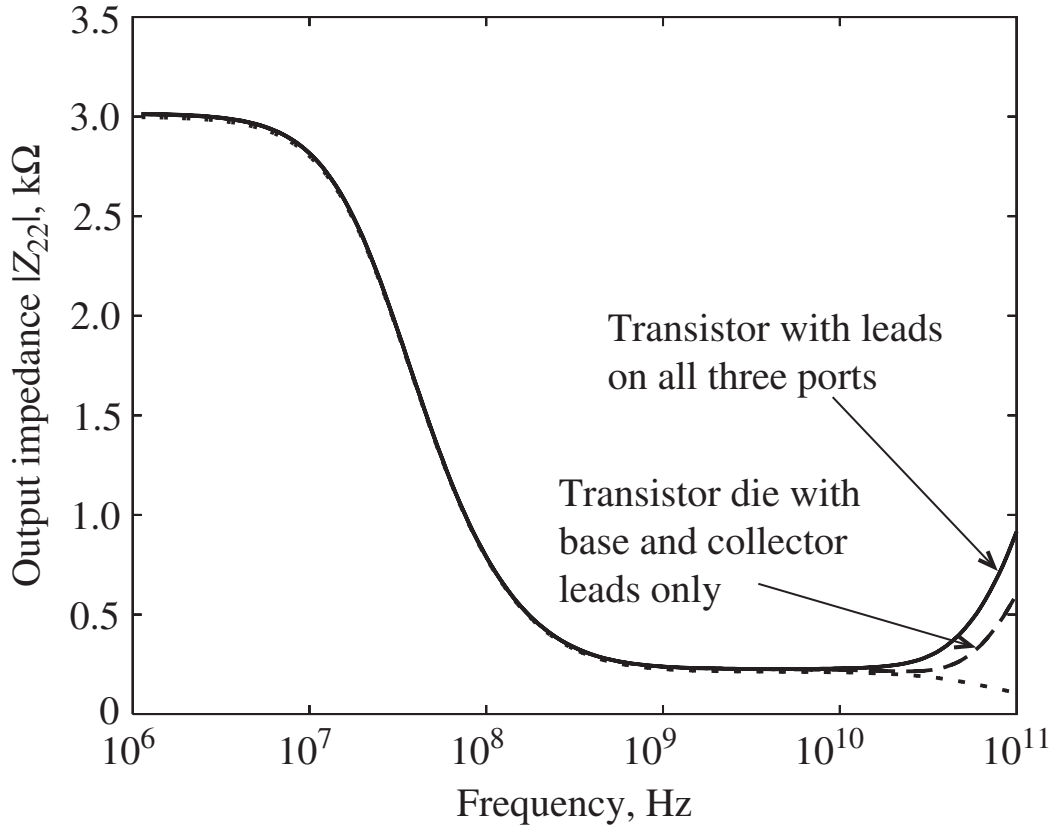


Figure 7-20 Complete transistor model divided into four two-port networks.

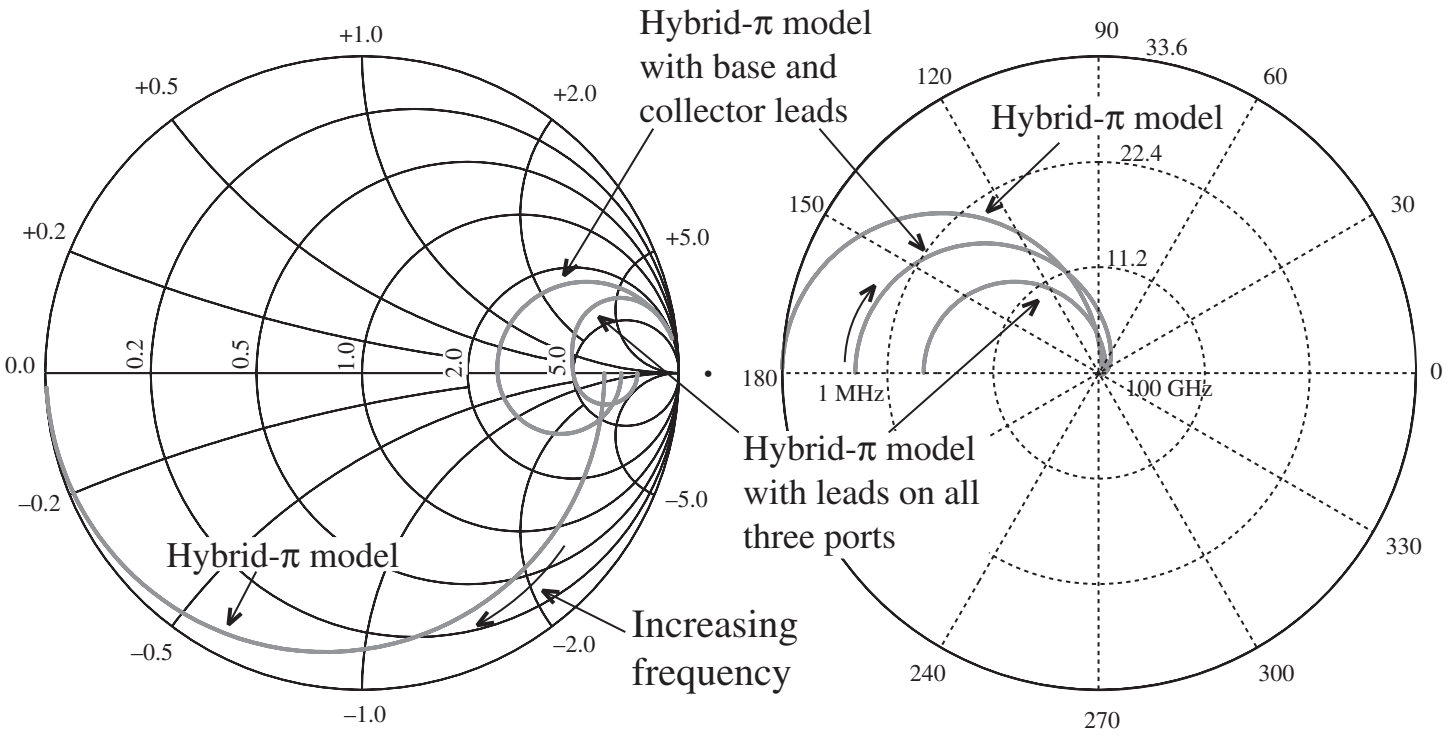


(a) Input impedance of the transistor



(b) Output impedance of the transistor

Figure 7-21 Input and output impedances as a function of frequency.



(a) Input reflection coefficient, S_{11} (b) Gain of the transistor, S_{21}

Figure 7-22 S_{11} and S_{21} responses of a BJT for various model configurations.

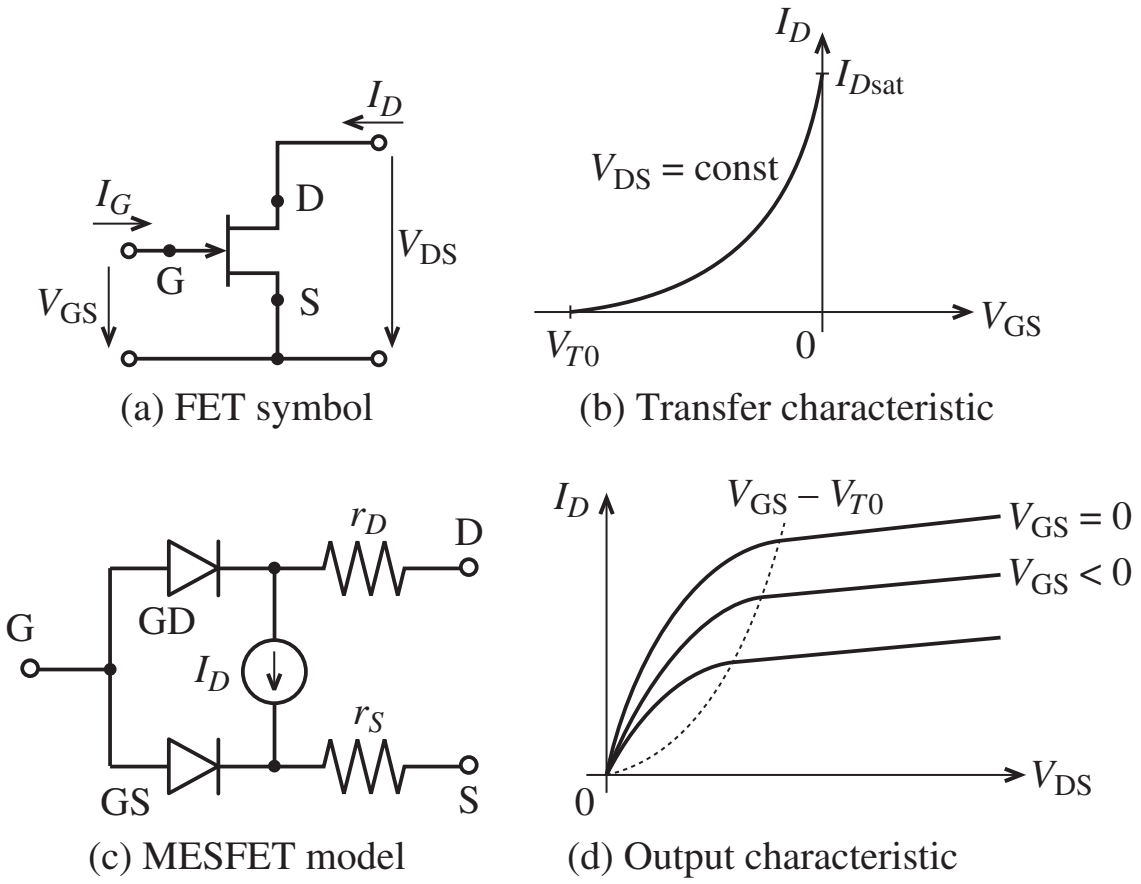


Figure 7-23 Static *n*-channel MESFET model.

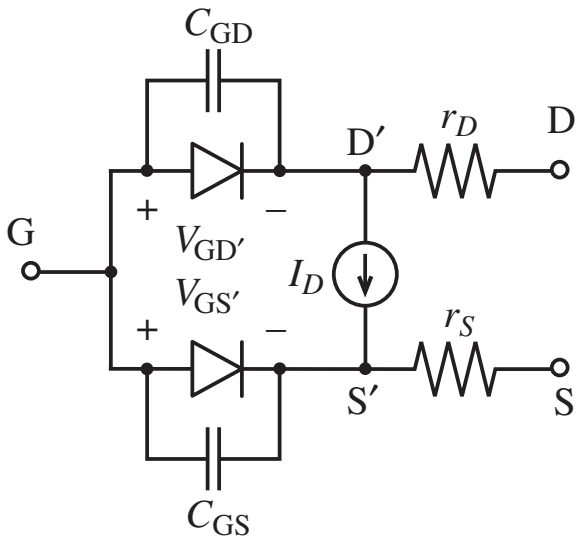
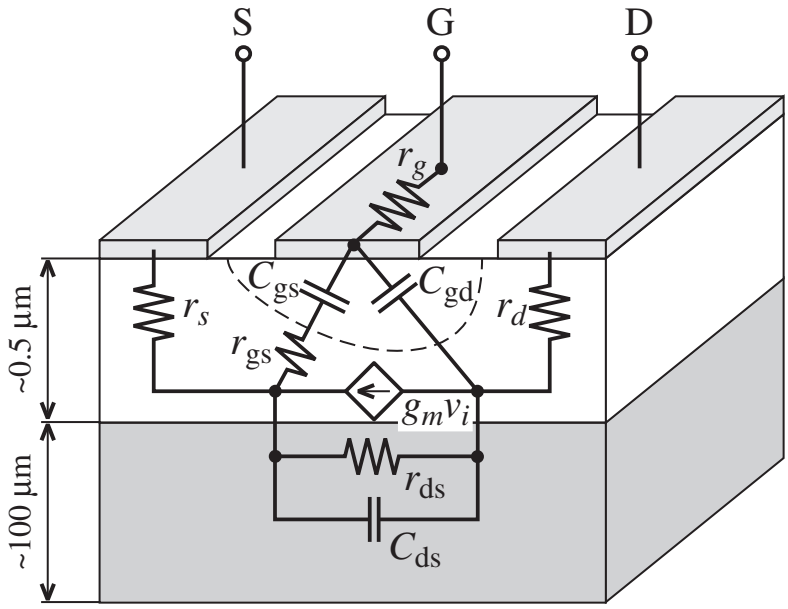


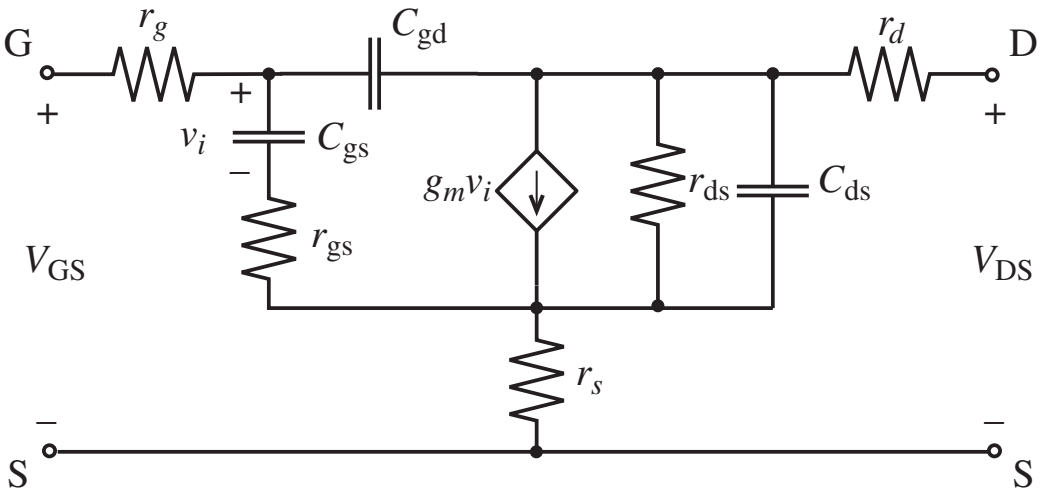
Figure 7-24 Dynamic FET model.

Table 7-4 SPICE modeling parameters for a MESFET

Symbol	SPICE	Description
V_{T0}	VTO	Threshold voltage
λ	LAMBDA	Channel length modulation coefficient
β	BETA	Conduction parameter
C_{GD}	CGD	Zero-bias gate-to-drain capacitance
C_{GS}	CGS	Zero-bias gate-to-source capacitance
r_D	RD	Drain resistance
r_S	RS	Source resistance



(a) Idealized MESFET device structure



(b) Circuit model

Figure 7-25 Small-signal MESFET model.

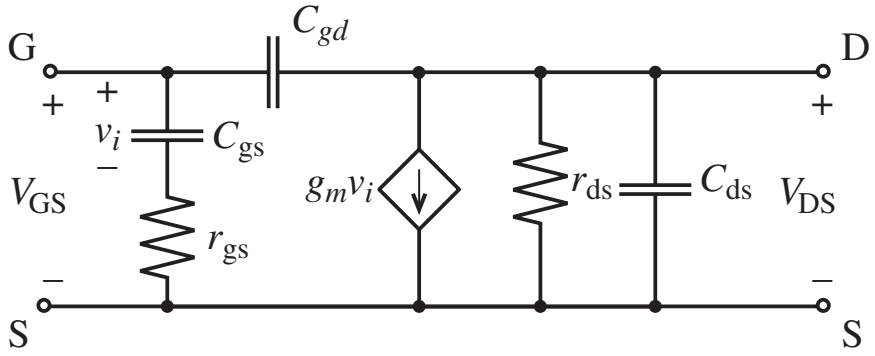


Figure 7-26 High-frequency FET model.

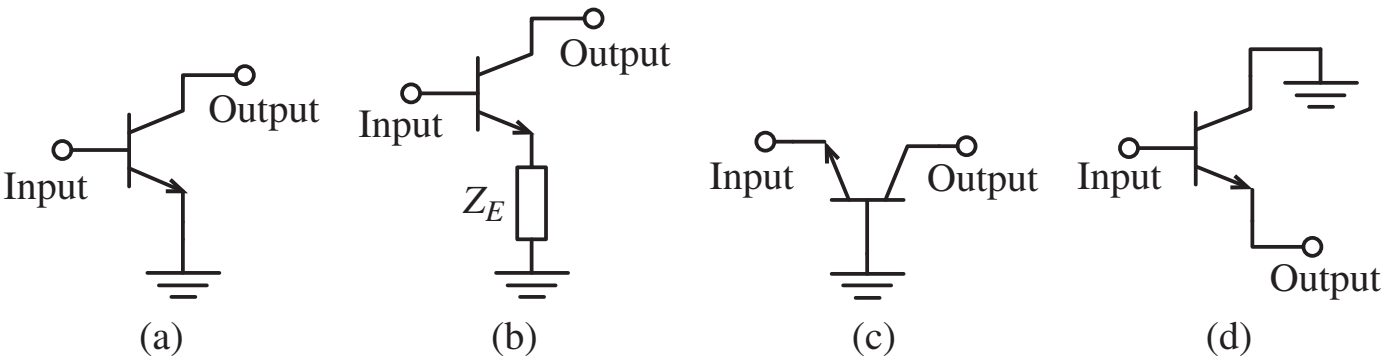
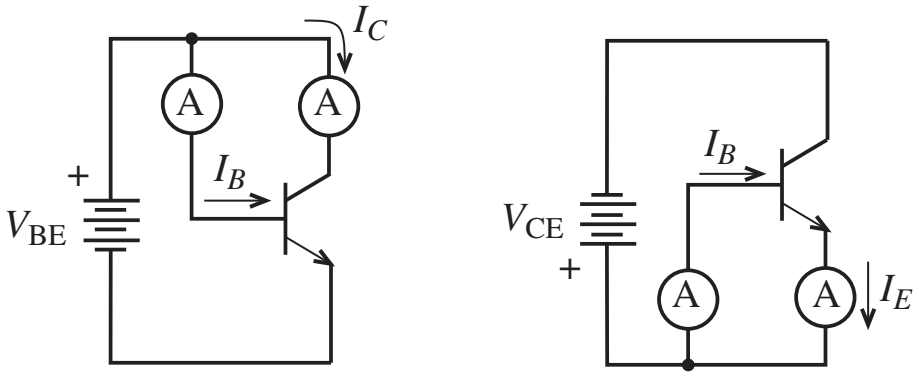


Figure 7-27 Single-transistor amplifier topologies: (a) common emitter (CE), (b) CE with emitter degeneration, (c) common base (CB), and (d) common collector (CC).

Table 7-5 Performance matrix of various single-transistor amplifier topologies

Topology	CE and CS	CE with emitter degeneration	CB and CG	CC and CD
Input impedance	High	$Z_{in\text{CE}} + (1 + h_{21})Z_E$ (inductive Z_E best)	$1/g_m$ (low)	$h_{21}Z_L$ (highest)
Voltage gain	$-g_m Z_L$ (high)	$-g_m Z_L/(1 + g_m Z_E)$ (lower than CE)	$g_m Z_L$ (high)	Near 1
Current gain	$-h_{21}$ (high)	$-h_{21}$ (high)	Near 1	h_{21} (high)
Output impedance	High	High	$\propto h_{21}Z_S$ (highest)	$1/g_m$ (low)
Reverse isolation	Fair (Miller effect reduces bandwidth)	Worse than CE (since feedback is present)	Good	Poor (but increases bandwidth)
Noise	Low	Higher than CE if resistive Z_E	Same as CE	High (output noise fed back into input)
Stability	Fair (Miller effect)	Somewhat better than CE	Good (but destabilized by feedback)	Poor (especially with capacitive load)
Linearity	Fair for BJT, good for FET	Better than CE (esp. for BJT)	Same as CE	Good if $Z_L > 1/g_m$



(a) Forward measurements (b) Reverse measurements

Figure 7-28 Forward and reverse measurements to determine Ebers-Moll BJT model parameters.

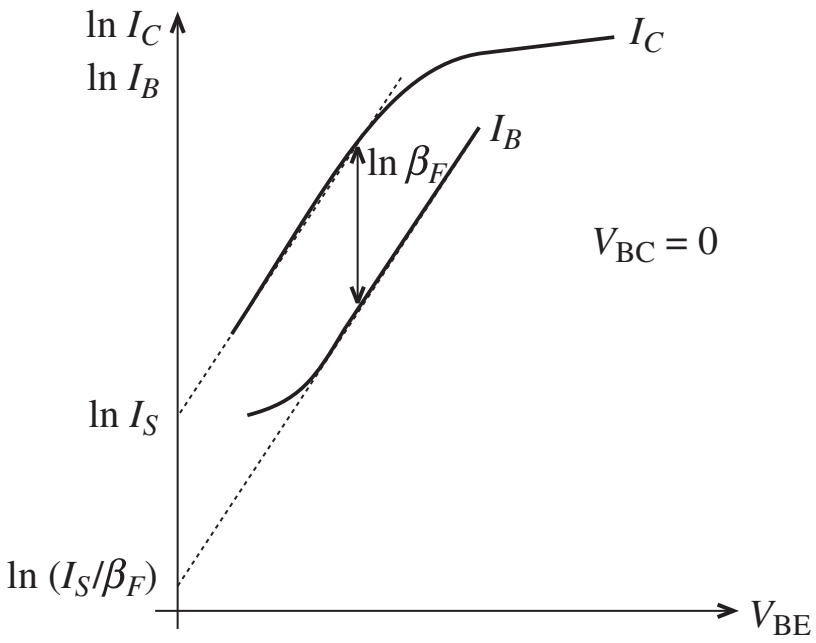


Figure 7-29 I_C and I_B versus V_{BE}.

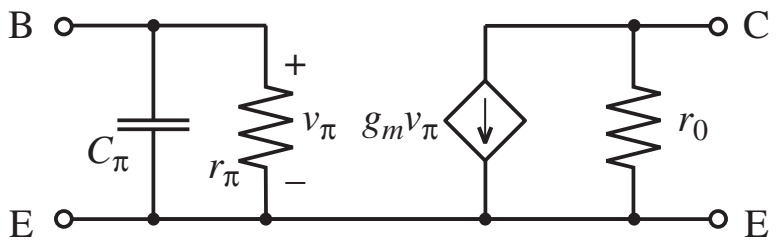


Figure 7-30 Small-signal, low-frequency model for parameter extraction.

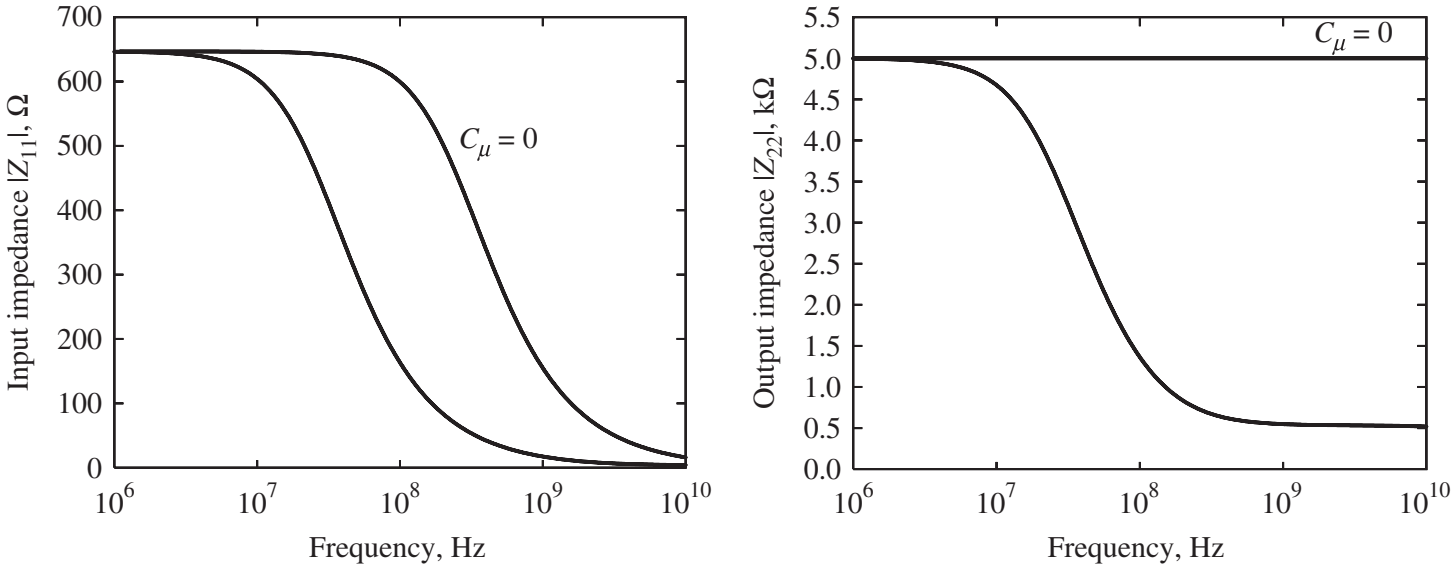
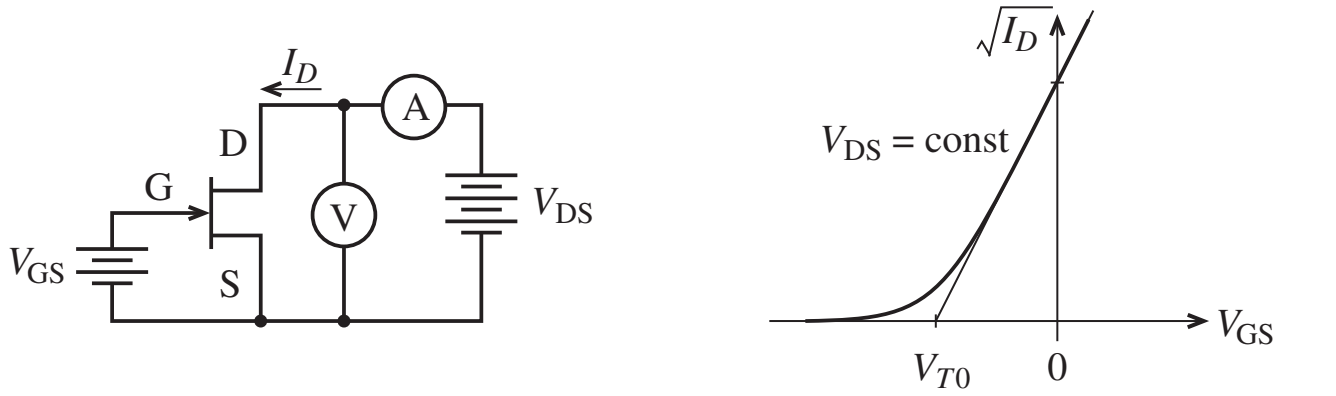


Figure 7-31 Input and output impedances with and without feedback.



(a) Measurement arrangement

(b) I_D versus V_{GS} transfer characteristic

Figure 7-32 Generic measurement arrangement and transfer characteristics in saturation region.

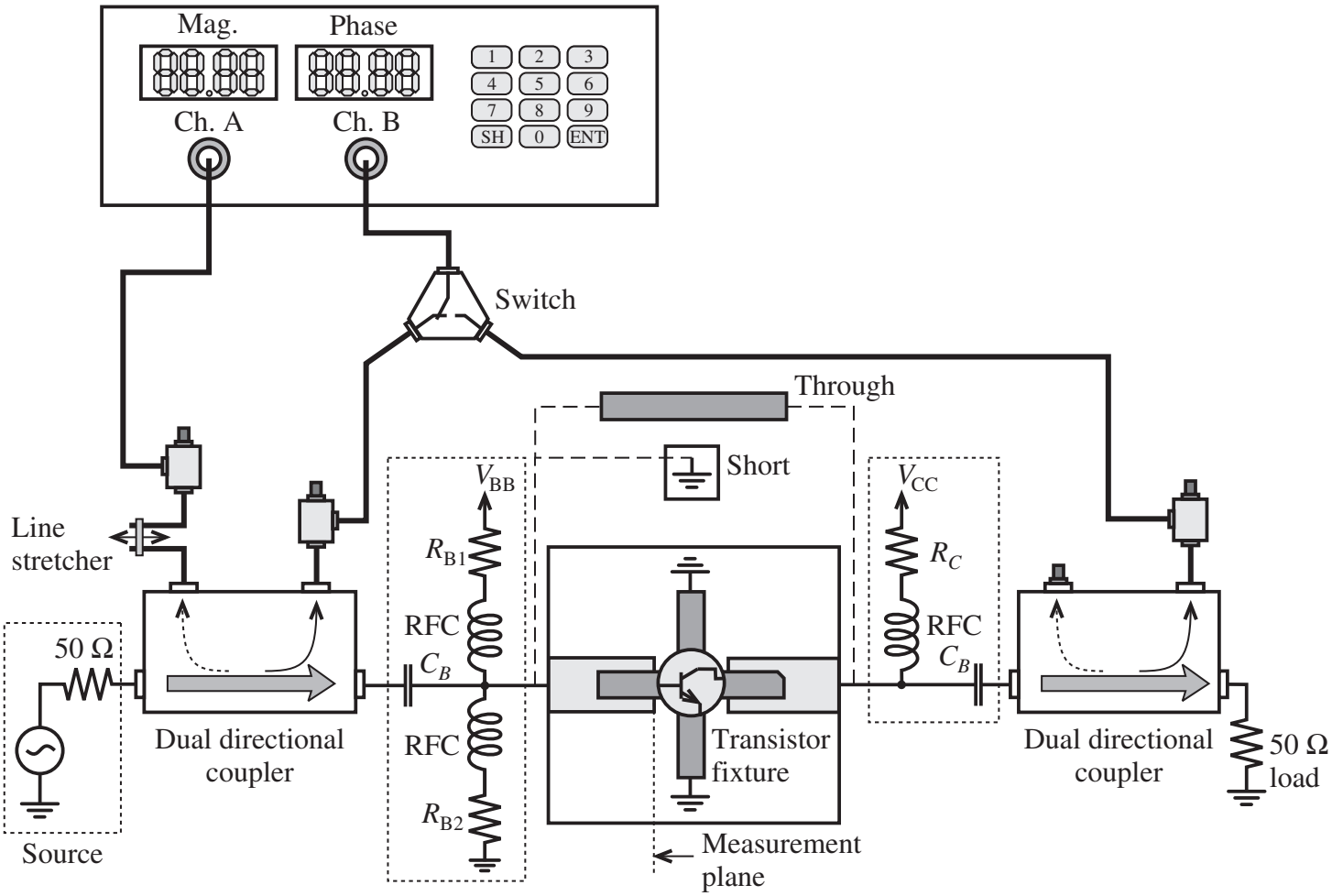


Figure 7-33 Recording of *S*-parameters with a vector voltmeter.

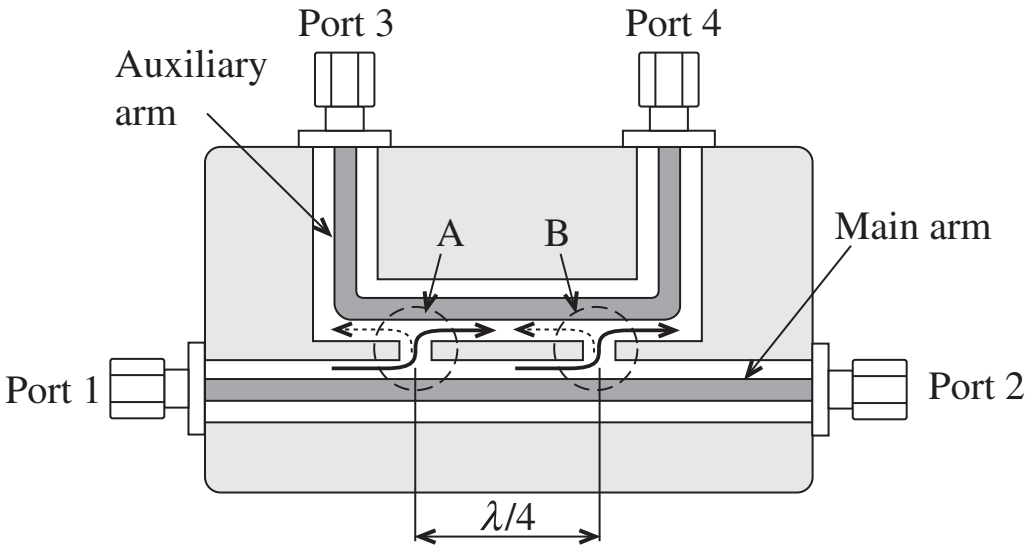


Figure 7-34 Cross-sectional view of directional coupler and signal path adjustment.

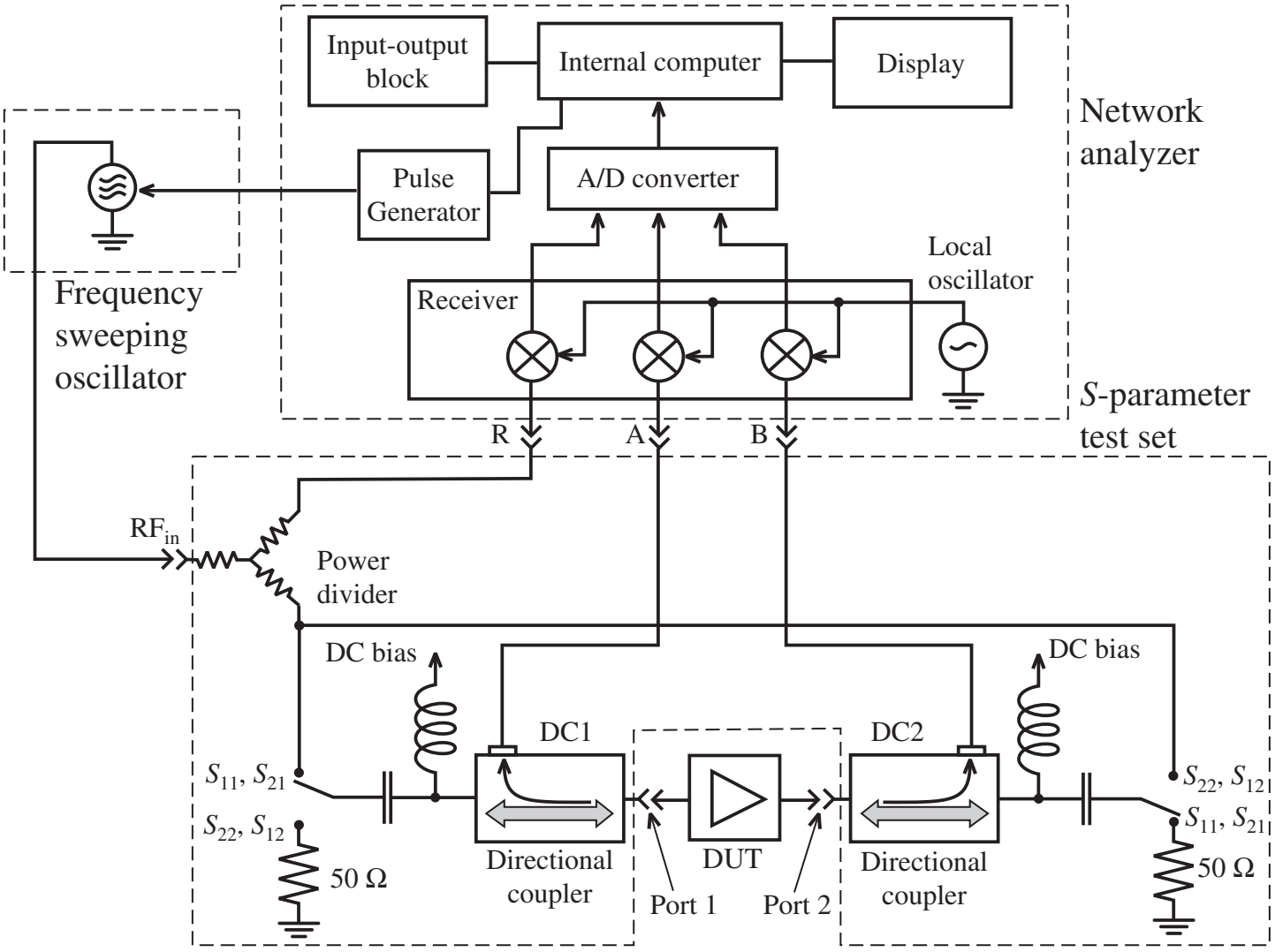


Figure 7-35 Block diagram of a network analyzer with *S*-parameter test set.

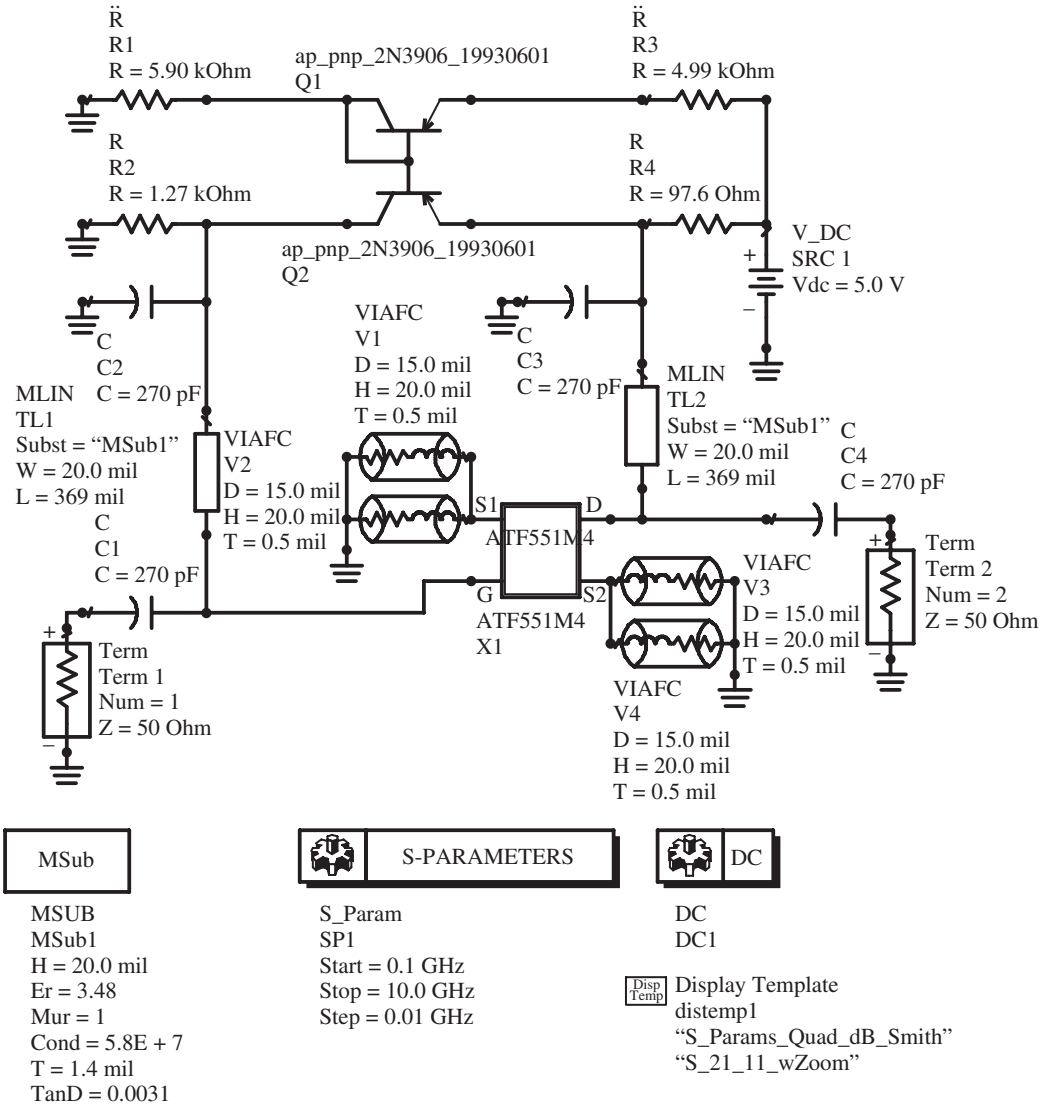


Figure 7-36 Circuit schematic of a 5 GHz amplifier with a HEMT device mounted on a simulated PCB with a biasing network and an *S*-parameter measurement setup.

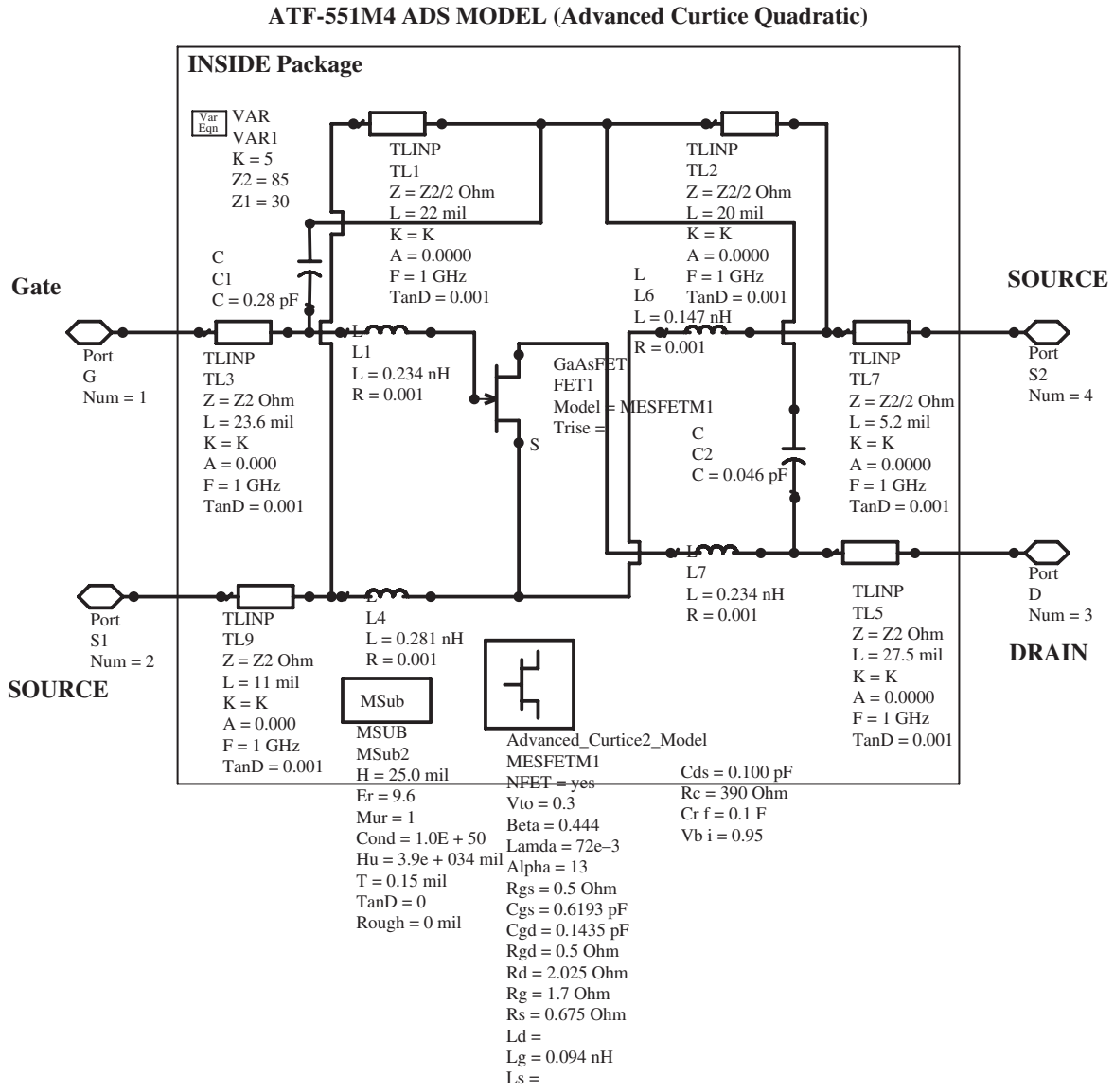


Figure 7-37 ADS circuit model for the HEMT including the transistor model and package parasitics.

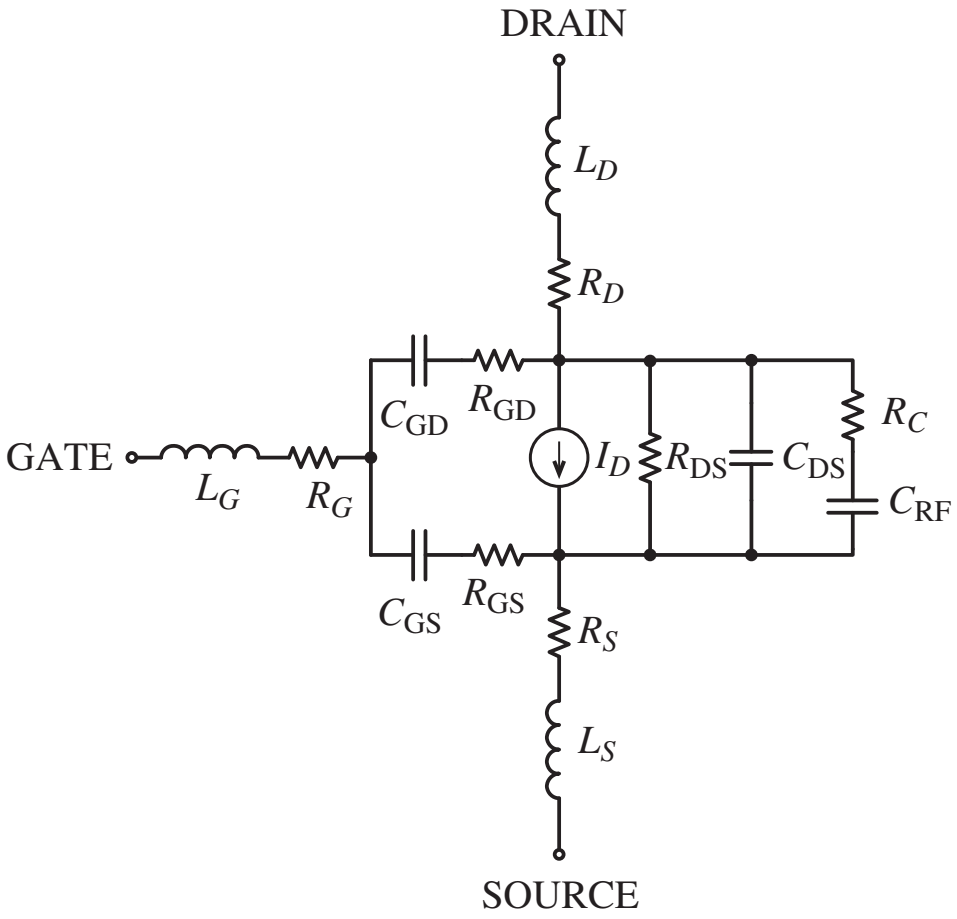
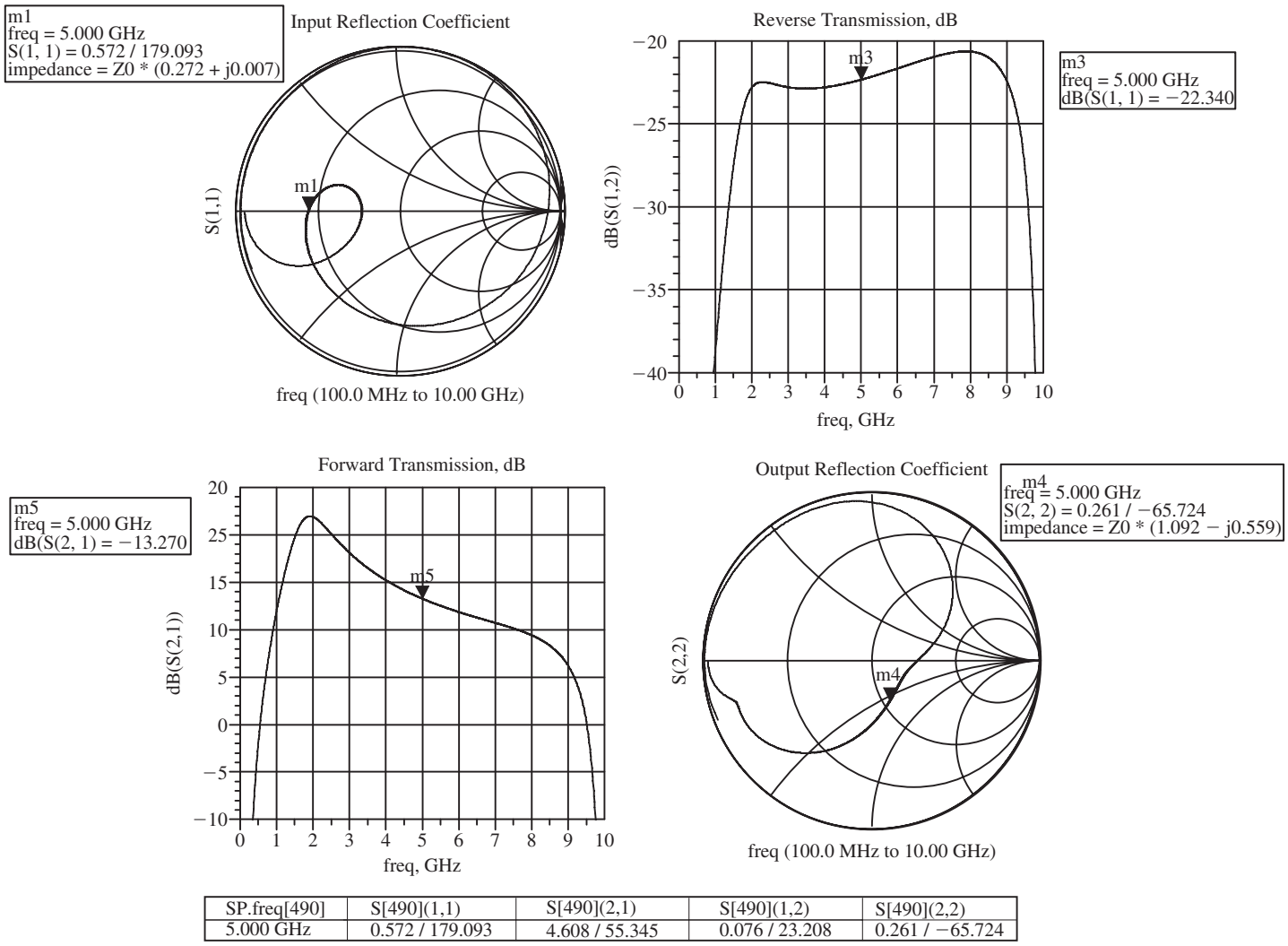


Figure 7-38 Basic circuit topology of the Curtice Quadratic GaAs MESFET model employed for the transistor die.



SP.freq[490]	S[490](1,1)	S[490](2,1)	S[490](1,2)	S[490](2,2)
5.000 GHz	0.572 / 179.093	4.608 / 55.345	0.076 / 23.208	0.261 / −65.724

Figure 7-39 ADS *S*-parameter sweep results for the 5 GHz amplifier.