Worcester Polytechnic Institute
Department of Electrical and Computer Engineering
ECE3311 – Intro to Communications B05

Exercise#4 An analog PLL

Introduction

Exercise #4 includes the understanding of basic operations and the hardware test of an analog PLL (DIP package) LM565CN. This PLL has a relatively low free-running frequency (up to 500 kHz, usually up to 380 kHz). It is used as FM/FSK/Coherent AM demodulator for voice signals and at the relatively low data rates. It is also used as a frequency synthesizer for low-rate modulation and demodulation.

If the chip is used as a demodulator, the low free-running frequency dictates the low IF (intermediate frequency) of the circuit, typically less than 300 kHz. Note that the standard IF for AM radio is 455 kHz; FM radio is using 10.7 MHz and higher IF's.

PLL's can be implemented in either digital or analog form. The analog PLL's are the only type capable of operating at high RF and microwave frequencies (Pozar, 2002).

1a. PLL circuit

A test PLL circuit around the PLL chip LM565CN is shown in Fig. 1. The VCO primary output is a square (not sinusoidal as in the textbook and lectures!) signal at pin 4 – the output of the relaxation oscillator on the base of the Schmitt trigger.

The square wave output shouldn't very considerably affect the loop performance since the square wave has the fundamental harmonic at a desired frequency and other harmonics are filtered out by the LPF.

The critical point now is how to close the PLL loop. From Fig. 1 one can see that the loop is closed if pin 4 (output of the VCO) and pin 5 (input to the phase detector) are connected together.

The "classic" phase detector of the PLL might include the mixer and the LPF, both on same chip. The practical realization is somewhat different. The National chip is using a circuit that is similar to the mixer as a phase detector.

1b. Low-pass filter

At the same time, the loop low-pass filter is made partially external. The RC LPF for LM565 is defined by the internal resistor $R_1 = 3.6\,\text{k}\Omega$ between pins 7 and 10 and an external capacitor C_1 between the same pins. If one chooses $C_1 = 0.1\mu F$ then the filter cutoff (3 dB) frequency will be

$$\frac{1}{2\pi R_1 C_1} = 442\ \text{Hz} \qquad (1)$$

Other LPF's (integrators) are possible. In the modern National chips the loop filter is usually made external to the chip or, in some cases, is made integrated (e.g. LMX2502). The loop filter affects two important PLL characteristics:

- Loop capture bandwidth
- Switching time.

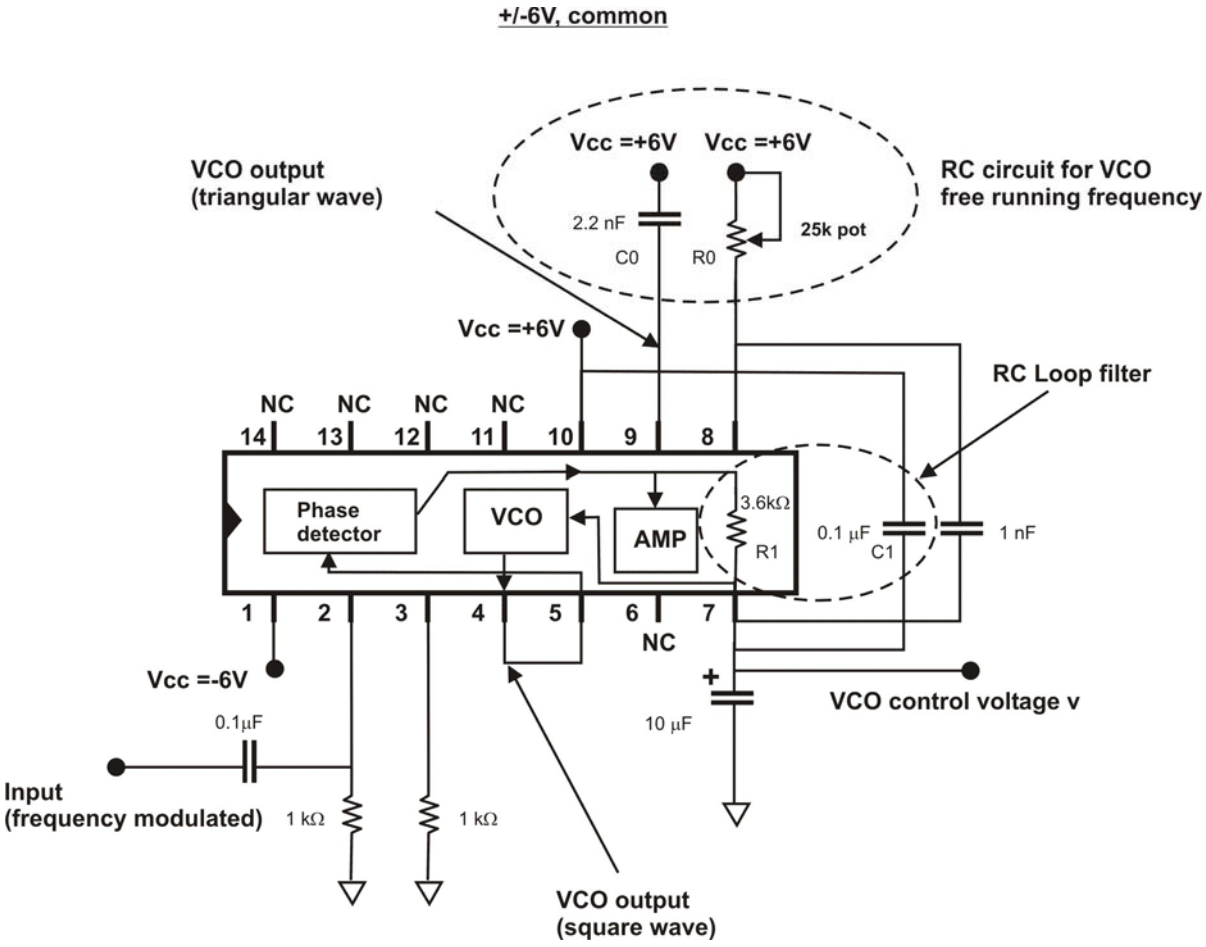

Fig. 1. A test circuit around the LM565 low-frequency analog PLL.

2. Measurement #1 – *free running frequency*

Set up the circuit as shown in Fig. 1 and connect it to the dual power supply (±6V, common). Don't forget the 10 μF cap from pin 7 to common. Make sure the PLL chip is placed in the middle of the protoboard. Connect channel 2 of the oscilloscope (AC coupled) to the oscillator output pin 9. In contrast to pin 4, pin 9 outputs an integrated (and inverted) square wave – triangular wave – the secondary output of the VCO. You should see a non-distorted triangular wave on the screen. The frequency of this wave is the *free- running frequency* of the PLL.

The free running frequency for this chip is given by the external RC circuit

$$f_0 = \frac{0.3}{R_0 C_0} \quad [\text{Hz}] \qquad (2)$$

which includes a fixed capacitor of 2.2 nF and a variable resistor.

Varying the resistor value determine

1. *Maximum possible free-running frequency for the circui.*
2. *Minimum possible free-running frequency for the circuit.*

What can you say about the signal distortion at the highest free-running frequency? After these measurements are complete, set up the free-running frequency at approximately 100 kHz. You will not change the free-running frequency anymore. This will be the IF frequency of the entire demodulator.

3. Measurement #2 – *hold-in (lock) bandwidth*

Connect the function generator to the circuit input (function generator ground is connected to common). Connect channel 1 of the oscilloscope to the circuit input. Turn the function generator on. Adjust the amplitude of the input harmonic (sine wave) oscillation to approximately 3 V. The frequency of the input signal should be 100 kHz. You should see two synchronized signals on the oscilloscope screen: one is the harmonic input (channel 1) and another is the triangular wave –output of the VCO (channel 2). Both channels should be AC coupled. Shift one of the signals up or down if they overlap.

Both signals should have exactly the same frequency – 100 kHz. Make sure that you simultaneously measure frequency for both signals.

But both signals also have the relative phase shift of 180 deg.

1. *Can you explain this effect? Based on the fact that the triangular wave at pin 9 is the inverted integral of the square wave – output to the VCO?*
2. *To do so you may want to check the phase relationship between the real VCO output – pin 4 or 5 and the external (input) signal. Now, is the VCO signal really leading the input signal by 90 degrees as predicted by theory (see lecture #11 where the VCO signal (cos) is leading the input signal (sin) by 90 deg)?*

Now tracking begins:

1. Rotate very slowly the frequency knob of the function generator and increase the input frequency. You should see on the screen that the VCO output *exactly* follows the input signal: the VCO frequency increases at the same rate. Also, the phase (or the relative phase difference) remains the same. The frequency readings of both the channels are also *the same*! However, when you continue to increase frequency further, after a certain moment, the oscilloscope signals suddenly become blurry. The frequency of two channels is no longer the same. This means that the PLL is out of the *hold-in range*. Measure this critical upper frequency f_L^+ (index *L* stands for "lock").

2. Return to the input signal of 100 kHz and start to decrease the input frequency. Frequency tracking again takes place, but only up to certain frequency f_L^-. After that frequency tracking fails. This means that the PLL is out of the *hold-in range* again. Measure this critical lower frequency f_L^-.

Determine the total lock range (or, which is the same, the locking bandwidth B_L *)*

4. Measurement #3 – *pull-in (capture) bandwidth*

An amazing property of the PLL is that it locks into the external frequency only within the *capture* or *pull-in range* where the PLL acquires lock. This range is determined by the low-pass filter and will be much smaller than the hold-in range.

1. Starting with the input frequency of 25 kHz of the signal generator slowly increase the input signal frequency and carefully watch frequency of both channels. Determine the pull-in lower frequency f_C^- (index *C* stands for "capture"), which corresponds to the point where the PLL first starts tracking frequency of the input signal. The free running frequency of the PLL (or VCO) should be always 100 kHz.

2. Starting with the input frequency of 200 kHz slowly decrease the signal frequency. Determine the pull-in upper frequency f_C^+, which corresponds

to the point where the PLL first starts tracking frequency of the input signal.

3. *Now determine the ratio of the capture bandwidth to lock bandwidth*

$$\frac{f_C^+ - f_C^-}{f_L^+ - f_L^-} \tag{3}$$

and see how small it is in reality!

Doesn't this feature remind you a hysteresis – the phenomenon, which is rather typical for a *nonlinear* system? This observation leads us to the conclusion the real PLL is essentially a *nonlinear* circuit. Therefore the linear model studied so far in class (and also in the textbook) is only of limited use. Actually, the linear model can only be used for the *pull-in (or capture) range* of the PLL.

Note that the pull-in range is equally often called the *capture range* of the PLL (Pozar, Microwave and RF Design of Wireless Systems). Accordingly, the hold-in range is called the *lock range* (ibid).

5. Loop gain

The loop gain is determined by two factors:

K_d - detector gain factor (the gain or sensitivity of the phase detector, V/rad, e.g. the mixer)

K_o - VCO gain factor (the gain or sensitivity of the VCO, (rad/sec)/V).

Their multiplication gives the loop gain in the form

$$\text{Loop gain} = K = K_d K_o \quad [\text{Hz}] \tag{4}$$

The loop gain K has the units of frequency (Hz). Its physical meaning is best viewed when one notes that the loop acquisition time τ (time required for the output of the PLL to respond to the step change in input frequency) is given by (the first-order loop only!)

$$\tau \approx \frac{1}{K} \tag{5}$$

i.e. inversely proportional to the gain. National reports that the loop gain of the present PLL is given by

$$K = \frac{33.6\, f_0}{V_C} \tag{6}$$

where V_C is *total* supply voltage to the circuit.

Whereas the hold-in range is mostly determined by the loop gain, the width of the pull-in range is mostly determined by the LPF characteristics – see below.

6. Measurement #4 – *PLL as a frequency-to voltage-converter*

Return to the input signal of 100 kHz. Reconnect channel 2 of the oscilloscope to pin 7 of the PLL, which will give the VCO control voltage. Do not forget to switch CH2 coupling to DC. In the present configuration, the PLL will work as a *frequency-to-voltage converter*. Namely, the VCO control voltage υ will be directly proportional to the deviation of the frequency of the input signal *from the free-running frequency of the VCO*.

Note that in the present experiment the VCO control voltage measured vs. ground (common) will *decrease but not increase* with increasing the frequency of the input signal and will have a large DC offset. Such a behavior is of minor importance and is connected to the fact that the VCO and the input are considered matched when they actually are at quadrature, with a 90 deg phase difference between them.

For six input frequencies given below (lock bandwidth) measure the corresponding VCO control voltages (at pin 7 vs. ground) using the cursor function of the oscilloscope. Voltage scale should be 500mV/div or finer. Fill out Table 1 below.

Table 1. PLL as a frequency-to-voltage converter (hold-in range).

Input frequency, kHz	50	75	100	125	150

VCO control voltage, V					

and answer the following questions:

1. *Is the voltage response of the PLL a linear function of input frequency?*

2. *What is the (average) gain (V/Hz) of the present PLL as the frequency-to-voltage converter?*