Worcester Polytechnic Institute
Department of Electrical and Computer Engineering
ECE3311 Principles of Communication Systems /B05
Exercise#3
Envelope detector with zero bias

I. Introduction

1.1. Small-signal diode model

Fig 1 shows the equivalent circuit for the Agilent HSMS-285x zero bias Schottky diode. The zero-bias diode is a low barrier Schottky device formed on p-type silica. The p-type offers the lowest possible cost, size, and complexity. Therefore, this diode is well suited for the mass production applications such as, for example, the RF ID tags[1,2].
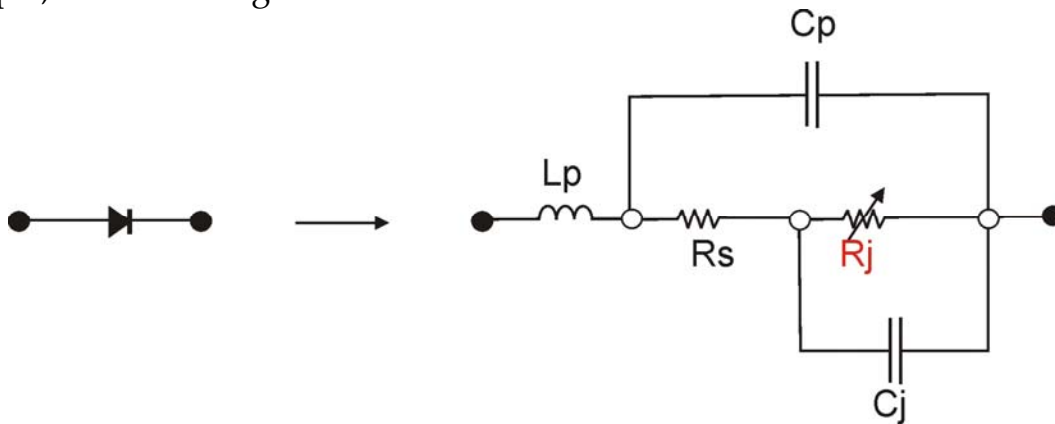

Fig. 1. Equivalent small-signal model of the diode including package parasitics.

Here[2] (see the reference in the footnote and the HSMS-285x family data sheet):

1. Lp – parasitic (package) inductance; Lp=2.0 nH
2. Cp – parasitic (package) capacitance; Cp = 0.08 pF
3. Rs – series parasitic resistance representing losses in the bondwire, etc., Rs=25Ω
4. Cj – junction capacitance, Cj = 0.18 pF
5. Rj – the most important diode parameter – junction resistance.

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[1] Agilent Technologies. Application Note 1089. Designing detectors for RF/ID tags. 1999.
[2] Agilent HSMS-285x Series surface mount zero bias Schottky detector diodes- Datasheet, 2005.

At 920 MHz, the corresponding impedances are:

1. Z(Lp) $= j11\ \Omega$
2. Z(Cp) $= -j2160\ \Omega$
3. Z(Rs) $= 20\ \Omega$
4. Z(Cj) $= -j961\ \Omega$

Rj (given in Ohms) depends on the applied bias current and given by (see Ref. 1)

$$R_j = \frac{0.026}{I_T}, \quad I_T = I_S + I_B \tag{1}$$

where (all currents are in amperes)

I_T – the total diode current

I_S – diode saturation (zero bias) current, $I_S = 3\ \mu A$

I_B – diode bias current (external DC current applied to the diode). Thus, Rj characterizes diode nonlinearity.

1.2. Diode detector

With or without external DC bias, Schottky diode detector circuits can be used to create low cost RF and microwave receivers with a sensitivity from -55 dBm to -57 dBm (see [2]). These circuits can have a variety of forms but in the simplest case they are equivalent to the book envelope detector circuit shown in Fig. 2.
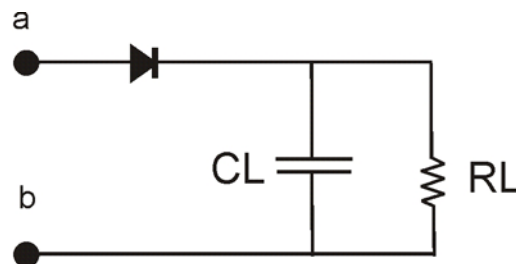

Fig. 2. Basic schematic of the envelope detector.

Here, RL is called the load resistance (or sometimes the video output resistance) and CL is called the load capacitance. The typical values used in envelope detectors are [1, 2]

RL = 100 kΩ
CL = 100 pF

This gives at 920 MHz:

Z(RL) = 100 kΩ
Z(CL) = -j1.7 Ω.

II. Matching impedance for unbiased diode detector

2.1. Input impedance of the envelope detector

The unbiased diode detector is the simplest one. However, when I_B =0 then Rj has a relatively high value,

Rj ≅ 9000 Ω

This makes the matching problem really complicated. Using the results of this and previous sections one can find the input impedance to the envelope detector circuit shown in Fig2. Combining circuits in Fig. 1 and Fig. 2 one obtains:

$$Z_{detector} \approx 60\Omega - j650\Omega \tag{2}$$

Amazingly (or may be not – just a good company's work!), the diode resistance appears to be almost 50Ω at 920 MHz! However, there is a very significant reactive (capacitive) part of about 650Ω that creates a problem.

2.2. Matching input impedance

Fig. 3a shows the naive diode detector circuit, without the impedance matching. The antenna (RF source with 50Ω input impedance) is directly connected to the diode detector. Fig. 3b shows the matched diode detector – matching is the simplest in this case - the series chip inductor is introduced to compensate for capacitance. We ignore the non-ideal impedance match for the resistance.
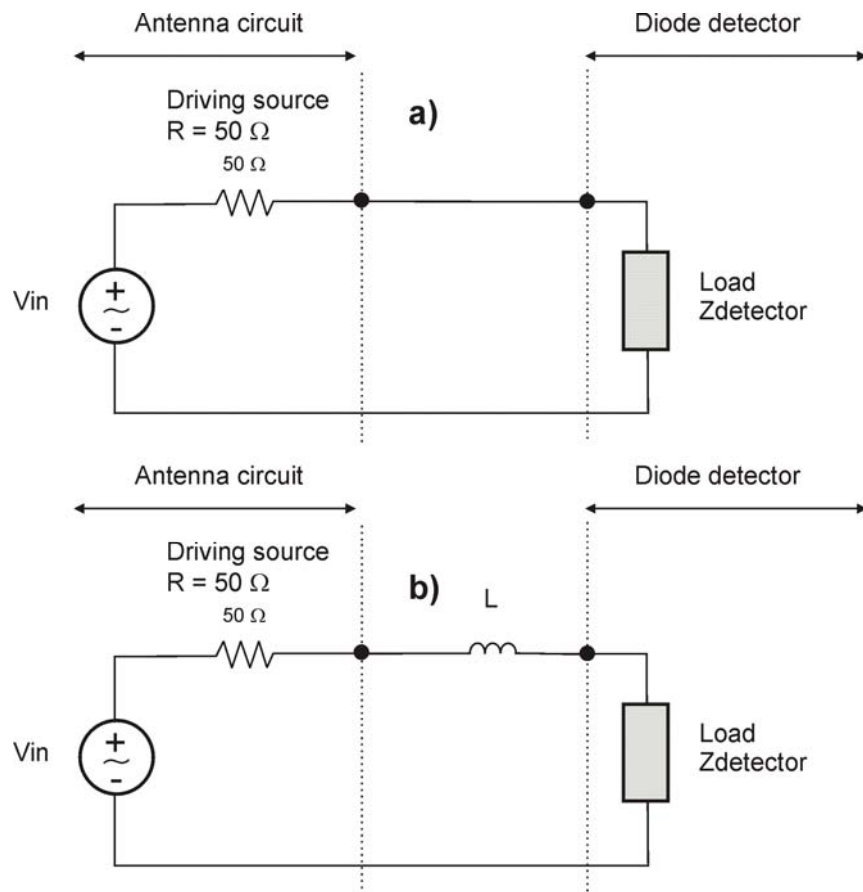
Fig. 3. Simplest impedance matching for the diode detector.

Let us assume that Vin has the peak-to-peak value of 2 mV. Please, calculate power delivered to the diode detector in both cases: with and without impedance matching, and record these values in your notes.

PLoad(without matching)   =

PLoad(with matching)   =

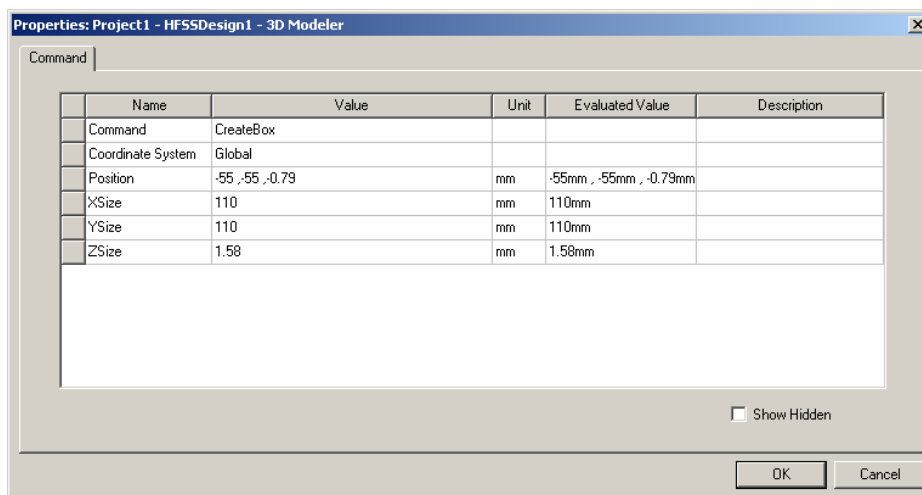How much power do we loose due to improper impedance matching (in dB)?

 Ploss(dB)   =

What is the inductor value that is needed at 920 MHz (in nH)?

L   =

2.3. Experiment #1 – impedance matching with a discrete component in ANSOFT.

1. Open Ansoft HFSS. Change both Project directory and Temporary directory to C:\temp (if necessary). Save the (empty) Ansoft project as Project3.

2. Introduce the dielectric substrate (62 mil FR4) by drawing the box with the size 110x110x1.58 mm. Center the box about the origin as shown in the dialog window below.

Name	Value	Unit	Evaluated Value	Description
Command	CreateBox			
Coordinate System	Global			
Position	-55 ,-55 ,-0.79	mm	-55mm , -55mm , -0.79mm	
XSize	110	mm	110mm	
YSize	110	mm	110mm	
ZSize	1.58	mm	1.58mm	

Properties: Project1 - HFSSDesign1 - 3D Modeler
Command
☐ Show Hidden
OK   Cancel

3. Open the material selection list (by using the right mouse click on the selected object). Assign FR4 material to that box.

4. Introduce the PEC ground plane for FR4.

5. Create a rectangle corresponding to the 50Ω microstrip on the top of FR4 as shown in the dialog window below and assign the PEC boundary to it.

6. Create the feed (lumped port) to the microstrip on the edge of the patch (50Ω).

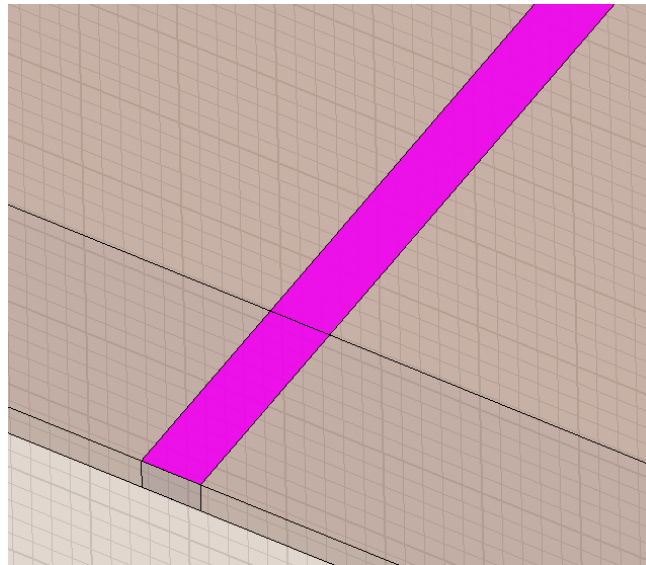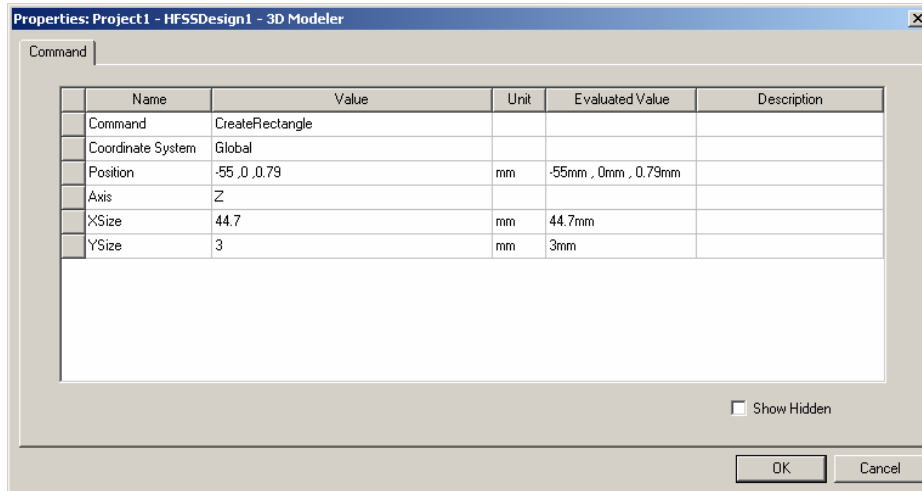|	Name	Value	Unit	Evaluated Value	Description
	Command	CreateRectangle			
	Coordinate System	Global			
	Position	-55 ,0 ,0.79	mm	-55mm , 0mm , 0.79mm	
	Axis	Z			
	XSize	44.7	mm	44.7mm	
	YSize	3	mm	3mm	

Fig. 4. Top – microstrip with the lumped port feed; bottom – microstrip rectangle.

7. At the end of the microstrip, draw a structure consisting of three rectangles – see Fig. 5. First rectangle will later model a lumped inductor (discrete load); second and third rectangles will model the diode package (or the whole detector circuit whose impedance is almost exactly the diode impedance) – also the discrete impedance load connected to ground.
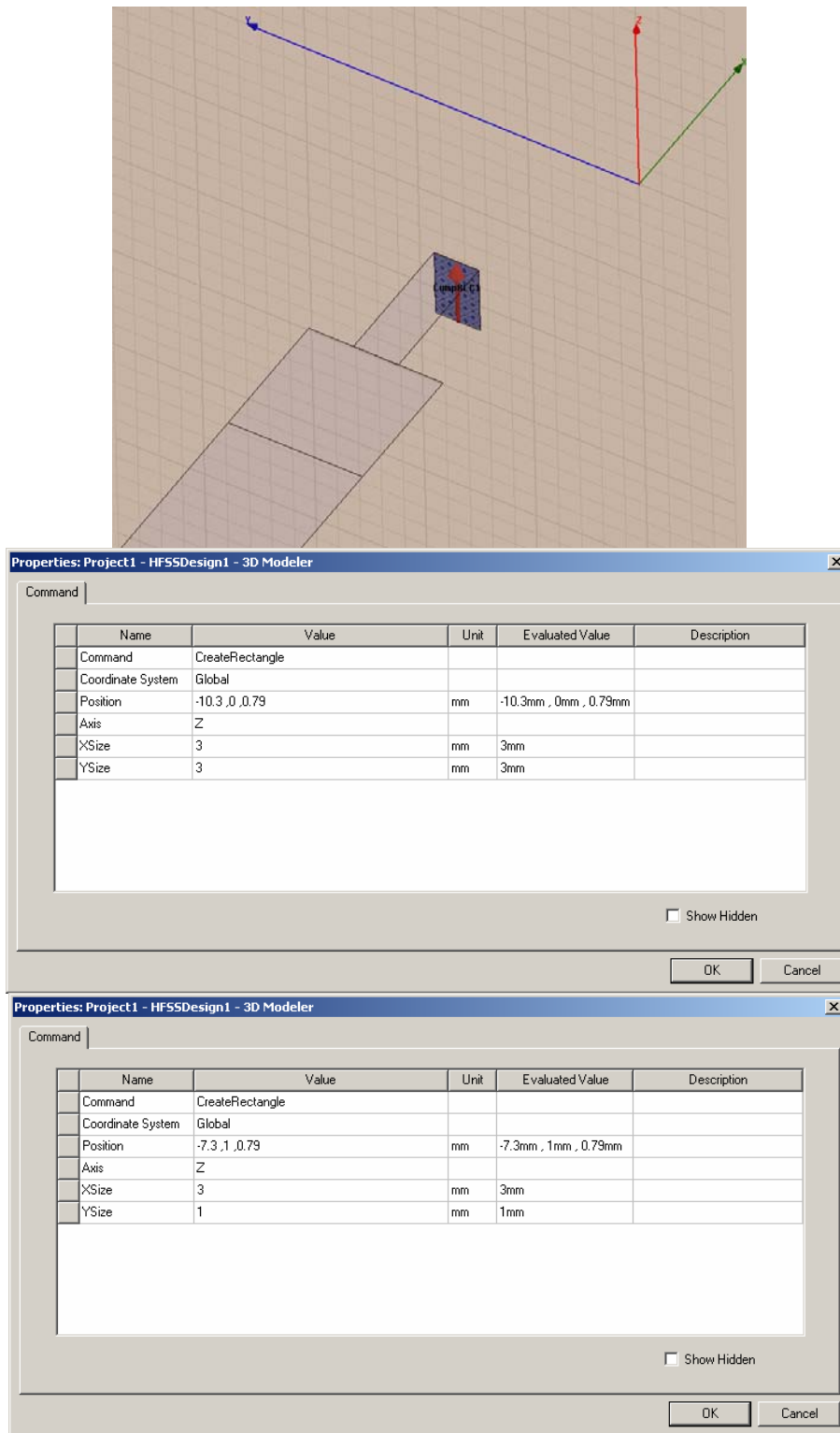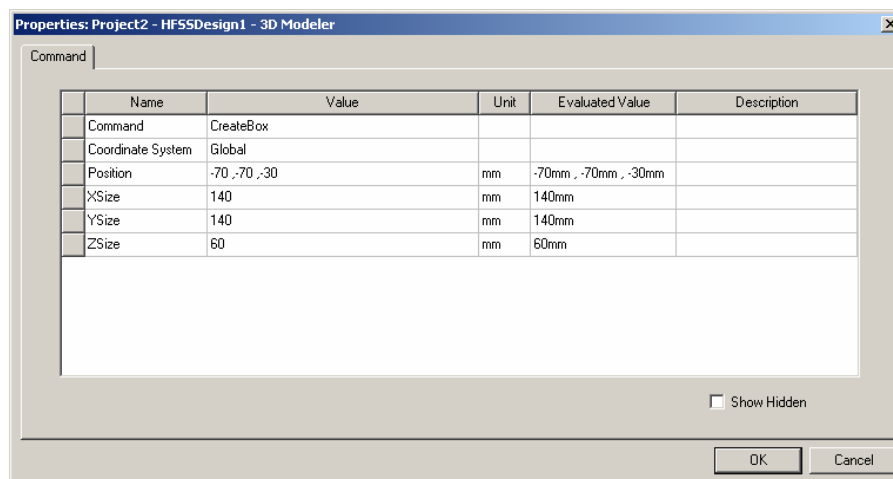
Fig. 5. Top – three-rectangle-structure at the end of the microstrip. First rectangle – lumped inductor (discrete load); second and third rectangles – diode or diode detector circuit (discrete impedance load connected to ground).
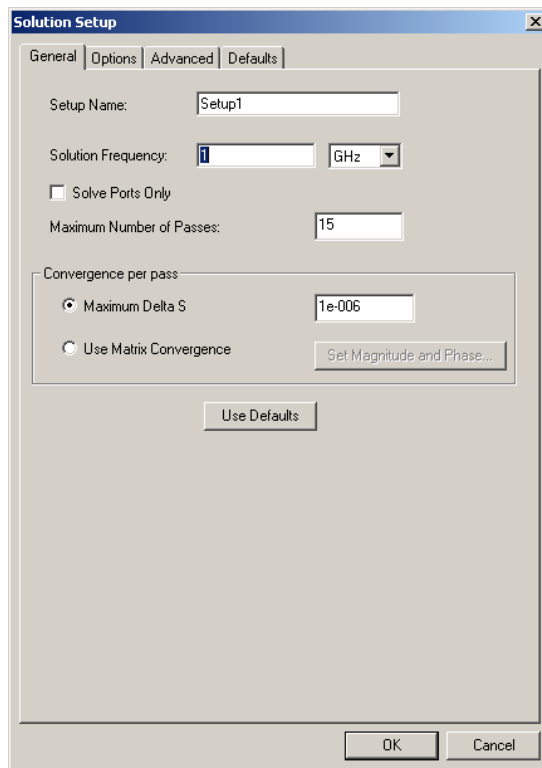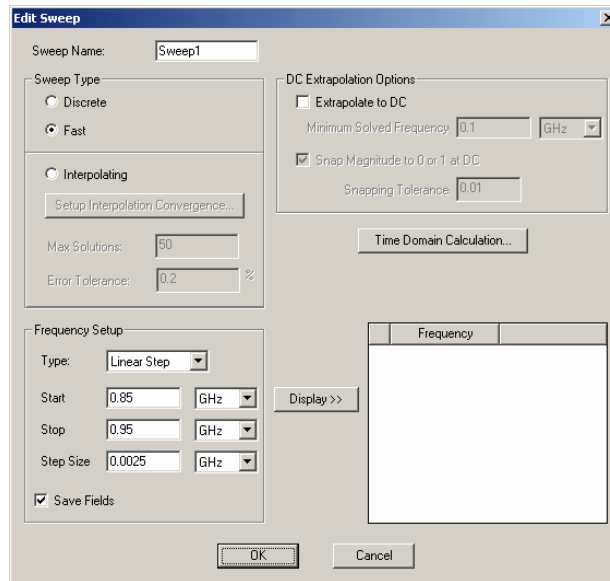
8. In order to test the circuit

i. assign the lumped RLC boundary (a lumped load) to the shorting connection to ground (to the vertical rectangle) with the pure resistance of 50Ω - terminate the structure into 50Ω load connected to ground. Do not forget to draw the current line along the rectangle – this is done similar to that for the lumped port.

ii. Assign the PEC to two remaining rectangles – the entire problem is thus reduced to a transmission line terminated to 50Ω load. One expects the reflection coefficient to be below – 20 dB.

9. Draw a larger (transparent) box around the entire structure as shown below and assign (right mouse click) the radiation boundary to it. We remember that assigning the closing boundary is necessary for any of the finite-element (FEM) simulations.

2.4. Simulation setup and results

The frequency sweep and simulation setup and should follow:

Edit Sweep dialog:

Edit Sweep

Sweep Name: Sweep1

Sweep Type
- ○ Discrete
- ● Fast
- ○ Interpolating

Setup Interpolation Convergence...

Max Solutions: 50
Error Tolerance: 0.2 %

DC Extrapolation Options
- ☐ Extrapolate to DC
  - Minimum Solved Frequency: 0.1 GHz
- ☑ Snap Magnitude to 0 or 1 at DC
  - Snapping Tolerance: 0.01

Time Domain Calculation...

Frequency Setup
Type: Linear Step
Start: 0.85 GHz
Stop: 0.95 GHz
Step Size: 0.0025 GHz
☑ Save Fields

Display >>

Frequency

OK   Cancel

Solution Setup dialog:

Solution Setup

General | Options | Advanced | Defaults

Setup Name: Setup1

Solution Frequency: 1 GHz

☐ Solve Ports Only

Maximum Number of Passes: 15

Convergence per pass
- ● Maximum Delta S   1e-006
- ○ Use Matrix Convergence   Set Magnitude and Phase...

Use Defaults

OK   Cancel

Finally, check your model (run validation check) and then start the simulations.

10. Plot the return loss of the circuit over the band. When the circuit is built correctly, the return it should go below -20 dB in the entire band. If this is

the case, plot your return loss (the so-called "Check" plot). Otherwise, debug the circuit.

11. Now, replace the 50Ω resistor to ground by 60Ω resistor. This will represent the real part of diode impedance from Eq. (2).

12. Assign the lumped RLC boundary to the second diode detector rectangle (the corresponding rectangle is highlighted below), with the impedance that is equal to

$$Z_{\text{detector}} \approx -j650\Omega \text{ at 920 MHz}$$

You may need to find the corresponding capacitance value first. Do not forget to assign the current line or current flow direction. Do not forget to remove the PEC boundary from the second rectangle!
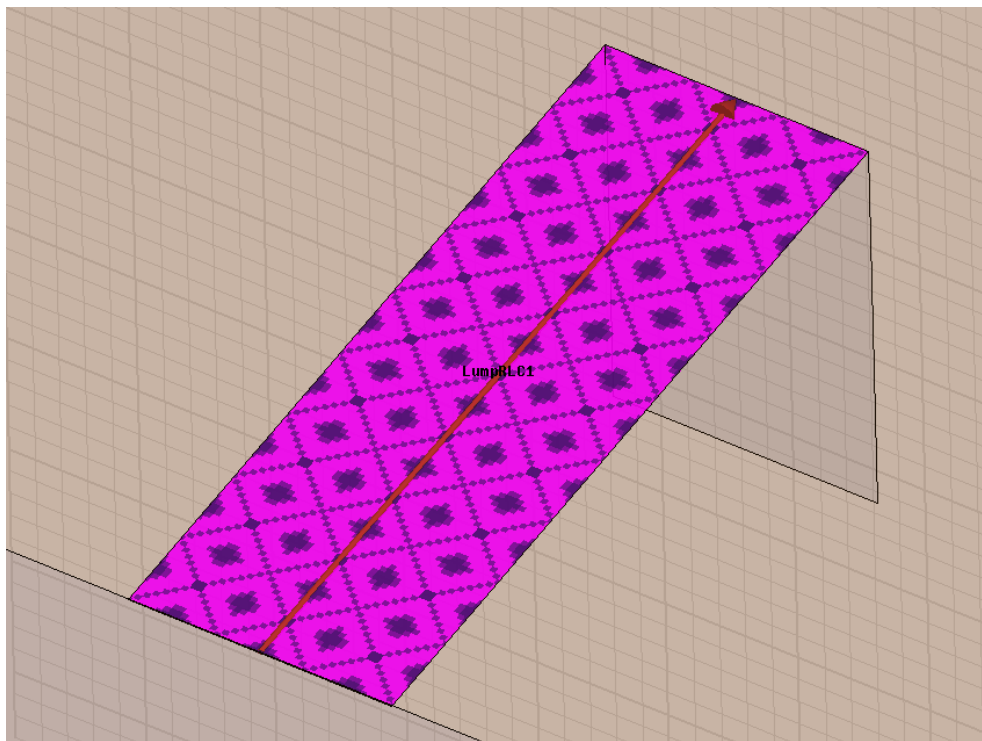
13. Keep the PEC definition for the first rectangle.

14. The present setup corresponds to Fig. 3a – no impedance matching. Run the validation check and, when no warnings appear, start the simulation.

The results should predict very poor values for the reflection coefficient – almost zero dB. If this is the case, plot your return loss (the so-called "No matching" plot).

15. Next, go to the last rectangle (closest to microstrip) in the chain and delete the PEC boundary. Instead, introduce the lumped inductance of 82 nH as shown below. Change frequency sweep to have a better resolution (shown below). Run the validation check.
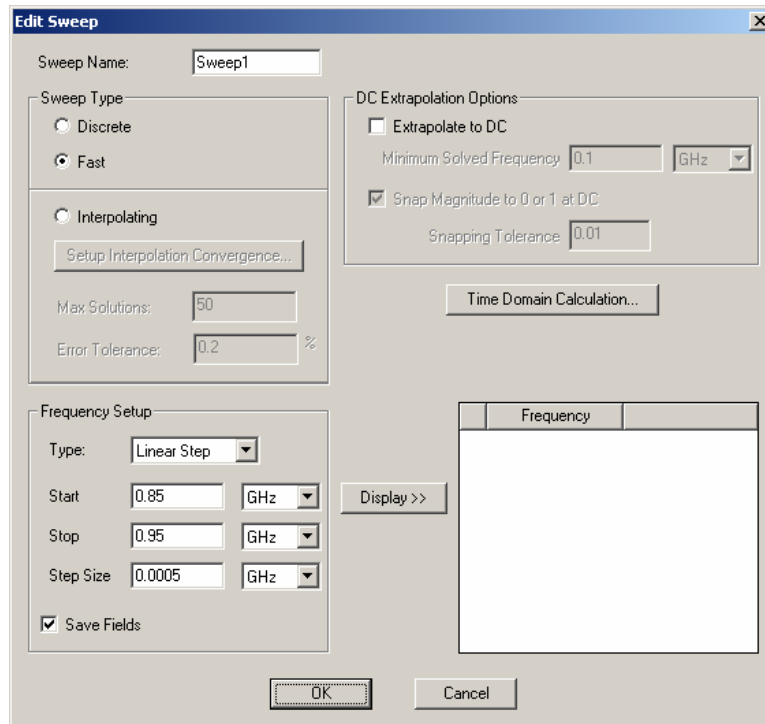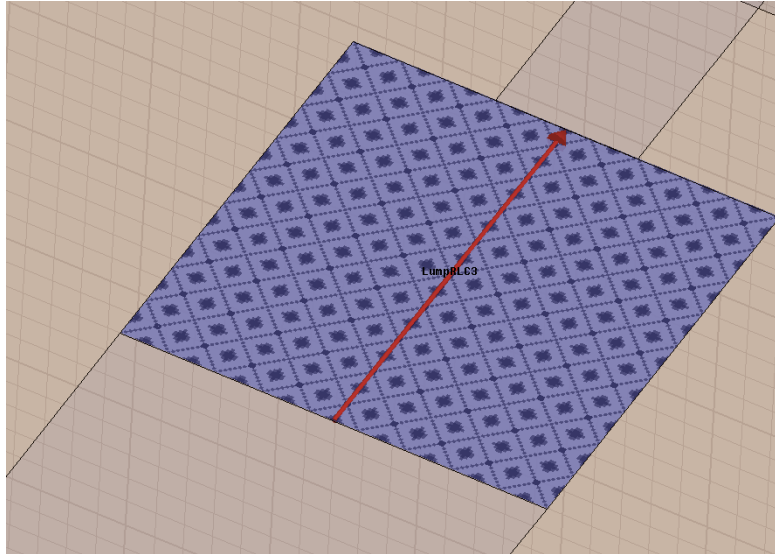
16. Run the simulation. The result should look like that shown in Fig. 6. If this is the case, plot your return loss (the so-called "Discrete-component matching" plot).

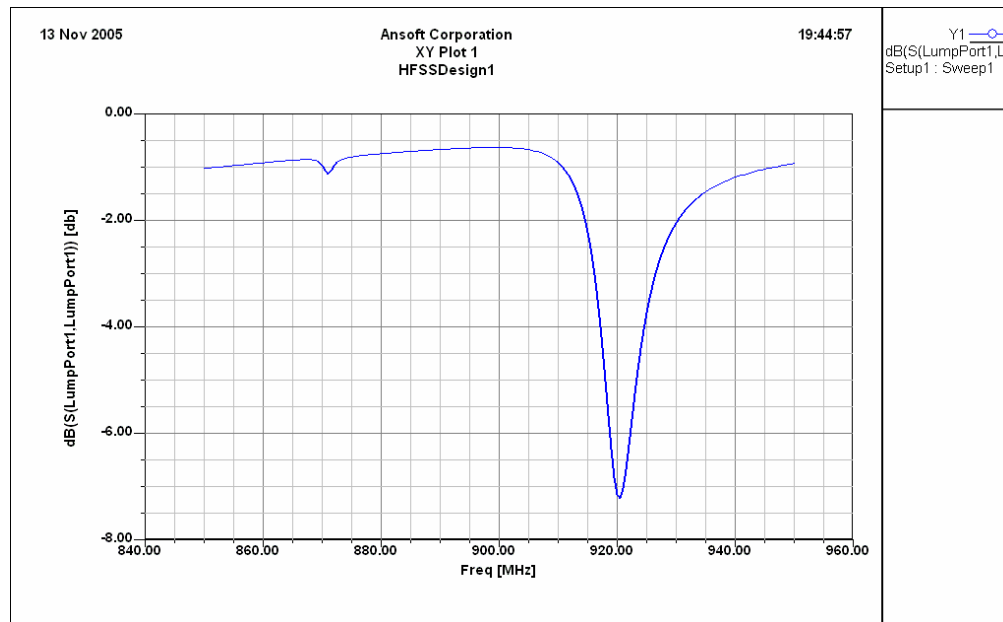

Fig. 6. The return loss of the diode detector matched with the lumped inductor.

III. Report

The report to this exercise should be attached to HW#3 on a separate sheet and it should be in the following format:

1. Answers to the questions on page 4.

2. Three plots: "Check" plot, "No matching" plot, "Discrete-component matching" plot.

3. How can you explain that the return loss in Fig. 1 is generally below 1 dB at any frequency? According to the power estimate it should be about -0.12 dB only. Do you think the ANSOFT simulations are correct?

4. Are you (honestly) satisfied with the (only) lumped inductor matching? What are major drawbacks of such matching[3]?

5. How can matching be really improved? Can you think about other diode detector possibilities? With a significant bias current (external DC current applied to the diode)? Keeping in mind that it is much simpler to match a load whose impedance is predominantly real and is reasonably close to 50Ω (say, in the range 50-300Ω)?

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[3] A more advanced matching circuit for the zero-bias Agilent diodes (RF/ID tags) is given in Ref. "Agilent HSMS-285x Series surface mount zero bias Schottky detector diodes- Datasheet, 2005". However, even this circuit may require fine inductor tuning.