Jitter in Phase-Locked Loops

John McNeill

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## Course Overview

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<td>• Design</td>
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## Basic Theory

- Original application: PLL clock recovery in SONET
- Example of jitter (time domain)
- Basic concepts: phase, jitter, modulation, phase noise
- Time domain, frequency domain characterization
- PLL refresher:
  - Loop dynamics, jitter source, noise model
- Characterization options:
  - Time/frequency domain figures of merit
  - Open/closed loop
- Measurement techniques / relationships
- Benefit of measurement relationships
Applications

• **Time Domain**
  – SONET / serial data communication
  – High Speed Clock Multiplication
  – Clock Distribution ("Zero Delay buffer")

• **Frequency Domain**
  – Wireless Communication
  – Oversampling ADC
  – Digital Audio
Practical Measurement Techniques

- **Time Domain**
  - Tektronix CSA803
  - Other techniques (Time Interval Analyzer)

- **Frequency Domain**
  - Spectrum Analyzer
  - Other Techniques (HP 3048 Phase Noise Analyzer)

- **Practical Measurement Techniques**
  - 50Ω interface
  - Signal integrity
  - Common pitfalls
Test Issues

- Observing nodes
- Testing multiple PLLs
- Self-test Issues
- Test choice issues
  - Time vs. frequency
  - Open loop vs. closed loop
- "Shortcuts" using measurement relationships
  - Time Domain
  - Frequency Domain
- Diagnostic tests
Design Techniques

• VCO Design using K figure-of-merit (time domain)
• Noise models for CMOS ring VCOs
• System level design issues
  – Loop bandwidth
  – Single-ended vs. differential
  – Delay Lock Loop (DLL)
• Other VCO design techniques
  – LC oscillator
  – Interference reduction techniques
  – Transient noise source simulation
  – VCO design in Frequency domain
## Basic Theory Overview

<table>
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<th>Measurement Techniques ↔ Design Tools</th>
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<td>• SONET Application</td>
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<tr>
<td>• Jitter / Phase Noise Fundamentals</td>
</tr>
<tr>
<td>• PLL Fundamentals</td>
</tr>
<tr>
<td>• PLL Noise Model</td>
</tr>
<tr>
<td>• Different Characterization</td>
</tr>
<tr>
<td>Techniques</td>
</tr>
</tbody>
</table>
Application and Requirements

- Serial data transmission over fiber optic link; requires:
  - Low bit error rate (BER)
  - Low cost, low power, simple interface
  - Recover bit clock from serial data
Clock Recovery with PLL

- **Advantage**
  - Low cost: entire system can be integrated
  - Requires integrated, low jitter VCO
Dynamic Phase Error (Jitter)

- Cycle-to-cycle variations in recovered clock
  - BER increases
  - Degrades performance in repeater applications
Jitter Referenced to Transmit Clock

TCLK

RCLK

$\sigma_X$
Measurement of Jitter Referenced to TCLK
### What is Phase?

- Phase is the argument of a trigonometric function:
  \[ V(t) = V \sin\left(\omega t + \phi\right) \]

- Frequency is the time derivative of phase:
  \[ \omega = \frac{d}{dt} \Phi(t) \]

- Phase is the integral of frequency:
  \[ \Phi(t) = \int_{t_0}^{t} \omega(t) \, dt + \phi \]
Time Domain Phase Characterization: Jitter

- Observed Voltage
- Phase
- Frequency

- $V(t)$
- $\Phi(t)$
- $\omega(t)$

- Frequency vs. Phase Observed Voltage

- Graphs showing time-domain representations of voltage, phase, and frequency over time.
Frequency Domain Characterization : Phase Noise

TIME DOMAIN

FREQUENCY DOMAIN

IDEAL SINE WAVE
AMPLITUDE NOISE
PHASE NOISE
Phase Noise: Modulation in Frequency Domain

Voltage / Time Error

Phase Error vs. Time

2-Sided Magnitude Spectrum

Phase Error

Magnitude Spectrum
Phase Noise: AM/PM Duality

SINE WAVE (IN QUADRATURE WITH CARRIER), AMPLITUDE MODULATED BY PHASE NOISE PROCESS

ADDED WITH CARRIER

PRODUCES PHASE MODULATED WAVEFORM (UNMODULATED CARRIER SHOWN FOR REFERENCE)
Phase Noise: AM/PM Duality

SINE WAVE (IN PHASE WITH CARRIER), AMPLITUDE MODULATED BY NOISE PROCESS

ADDED WITH CARRIER

PRODUCES AMPLITUDE MODULATED WAVEFORM (UNMODULATED CARRIER SHOWN FOR REFERENCE)

Caution: AM, PM Have Same Magnitude Spectrum!
Phase Noise: Sine Wave to Square Wave

Square wave from ideal sine wave: harmonics
Phase Noise: Sine Wave to Square Wave

Shape of phase noise near fundamental unchanged
Frequency Domain Measurement

- Equipment: Spectrum Analyzer
- "Direct Spectrum" Procedure
  - Feed clock into RF input
  - Observe spectrum near fundamental frequency
VCO Spectrum Measurements

- Phase noise spectrum “close in” to carrier
- 155.52 MHz carrier     1MHz span
Single-Sided (Phase Noise) Measurements

- Phase noise P.S.D. symmetric about carrier
- Just measure one side of spectrum
- Plot on log scale to show frequency structure
### PLL Noise Model / Loop Dynamics Refresher

- **Simplified noise model**
  - Dominated by white noise at VCO input
    (Or equivalent)
- **Open loop phase noise**
- **PLL response to VCO phase noise**
- **Phase noise at PLL output**
  - Shaped by loop dynamics
Simplified Noise Model

- Ideal VCO with white noise at input
Open Loop VCO Phase Noise

\[ \log S_{\text{Vctl}}(f) \]

\[ \log S_{\Phi}(f) \]

\[ \propto \frac{1}{f^2} \]

Vctl INPUT
WHITE NOISE p.s.d.

OPEN LOOP PHASE NOISE p.s.d.
(INTEGRATED WHITE NOISE)
PLL Response to Phase Noise

PHASE DETECTOR

Kd (θi - θo)

LOOP FILTER

F(s)

VCO

Ko

s

θn

θi

θo

θn

Hs(f) PHASE INPUT

\[ \frac{\theta_i}{\theta_n} \]

Hn(f) PHASE NOISE TRANSFER FUNCTION

\[ \frac{\theta_o}{\theta_n} \]

log f

f_L

log H(f)

McNEILL: JITTER IN PHASE-LOCKED LOOPS
Phase Noise at PLL Output

OPEN LOOP PHASE NOISE p.s.d. (INTEGRATED WHITE NOISE)

CLOSED LOOP p.s.d. (LOWPASS DUE TO SHAPING BY LOOP)

LOOP PHASE NOISE TRANSFER FUNCTION
Measurement Strategy Overview

• Relate different measurement techniques:
  – Open loop / closed loop
  – Time domain / frequency domain
  – Self referenced / transmit clock referenced
Jitter Referenced to Transmit Clock

TCLK

RCLK

$\sigma_X$
Measurement of Jitter Referenced to TCLK
TCLK-Referenced Time Domain Measurement

• Advantages
  – “Compresses” noise performance into one number
  – CSA time base accuracy not critical

• Disadvantages
  – Requires stable source for PLL lock
  – Requires access to transmit clock
  – “Compresses” noise performance into one number
    • Little or no information on noise process
    • Shape of histogram (maybe)
Time Domain: Two sample standard deviation

- Equipment: Communications Signal Analyzer (CSA)
- Procedure
  - "Self referenced:" clock is both trigger and input
  - Observe distribution of delay times to threshold crossings of clock
  - Plot $\sigma$ as a function of delay $\Delta T$

Average delay = $N\Delta T$
Open Loop VCO Time Domain Measurement

Open loop:
- Break PLL feedback loop by shorting input to VCO
- Tie to signal ground (constant voltage)
Open Loop VCO Time Domain Measurement

Open loop:
\[ \sigma \propto \sqrt{\Delta T} \]

\[ \sigma_{\Delta T(OL)}(\Delta T) \approx K \sqrt{\Delta T} \]

Model:
Period errors independent random variables

• Variance \((\sigma^2)\) of sum is sum of variances
• Standard deviation increases as square root

\[ K \]

Time domain figure-of-merit

\[ \text{Measured jitter} \]

Fit to
\[ \kappa = 6.14 \times 10^{-8} \sqrt{s} \]

Delay \(\Delta T \) [ns]
PLL VCO Time Domain Measurement: Closed Loop

- **Open loop:**
  \[ \sigma \propto \sqrt{\Delta T} \]
  \[ \sigma_{\Delta T(OL)}(\Delta T) \approx K \sqrt{\Delta T} \]

- **Closed loop:**
  Action of loop limits \( \sigma \) for delays longer than loop bandwidth \( \tau_L \)

\[
\tau_L = \frac{1}{2\pi f_L}
\]

\[
\kappa \sqrt{\Delta T}
\]

<table>
<thead>
<tr>
<th>Delay ( \Delta T ) [ns]</th>
<th>Predicted</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10000</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fit to
\[ \kappa = 6.14E-08 \sqrt{s} \]
<table>
<thead>
<tr>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Structure of $\sigma_{\Delta T}$ vs. $\Delta T$ plot gives information on noise process</td>
<td>- $\sigma_{\Delta T}$ fails to converge in presence of frequency drift (&quot;wander&quot;)</td>
</tr>
<tr>
<td>- Does not require access to transmit clock</td>
<td>- Limited by accuracy of CSA time base at long $\Delta T$</td>
</tr>
<tr>
<td>- Applicable to free running VCO (PLL open loop)</td>
<td></td>
</tr>
</tbody>
</table>
Frequency Domain Measurement

- **Equipment:** Spectrum Analyzer
- "Direct Spectrum" Procedure
  - Feed clock into RF input
  - Observe spectrum near fundamental frequency
PLL VCO Spectrum Measurements

Open loop:
spectrum proportional to $1/f^2$
(f = offset frequency from carrier)

$$S_{\phi OL}(f) \approx \frac{N_1}{f^2}$$

Model: Dominated by white noise at VCO input

- Carrier phase modulated by noise at VCO input
- Phase is integral of frequency

$N_1$
Frequency domain figure-of-merit
PLL VCO Spectrum Measurements

Open loop:
Integration of white noise at VCO input gives $1/f^2$ spectrum

$$S_{\phi OL}(f) \approx \frac{N_1}{f^2}$$

Closed loop:
$1/f^2$ spectrum shaped by loop filter
Spectrum rolls off for $f < f_L$

SPECTRUM ANALYZER PLOT
## Frequency Domain Measurement

<table>
<thead>
<tr>
<th>Advantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Simple and quick</td>
</tr>
<tr>
<td>- Most work on phase noise has been done in frequency domain</td>
</tr>
<tr>
<td>- Easy to see effect of loop filter on jitter</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>- This is not how the serial data communication customer decides whether the part is working!</td>
</tr>
</tbody>
</table>
Relating Different Jitter Measurements

- **Reason**
  - Design in the domain that gives the most insight
  - Always able to relate to end user's specification

- **Analysis Domains**
  - Time
  - Frequency

- **PLL Operating Conditions**
  - Closed loop
  - Open loop (stand alone)
Summary: (i) Frequency domain, VCO open loop

\[ S_{\Phi 1}(f) = \frac{N_1}{f^2} \]
Summary: (ii) Frequency domain, VCO closed loop

\[ S_{\Phi_{CL}(f)} \]

\[ f_L \]

\[ f \]
Summary: (iii) Time domain, closed loop, transmit clock ref

![Diagram]

- DATA SOURCE
- CLOCK RECOVERY PLL (D.U.T)
- COMMUNICATIONS SIGNAL ANALYZER

- TCLK
- TDATA
- RCLK
- RDATA
- TRIG
- VERT

- p(t)
- σx
- t
Summary: (iv) Time domain, closed loop, self referenced

\[ \sigma_{\Delta T(\text{CL})}(\Delta T) \]
Summary: (v) Time domain, open loop, self referenced

\[ \Delta T \]

\[ \sigma_{\Delta T(OL)}(\Delta T) \]

\[ \kappa \sqrt{\Delta T} \]
Measurement technique summary

<table>
<thead>
<tr>
<th>PLL CLOSED LOOP</th>
<th>FREQUENCY DOMAIN</th>
<th>PLL CLOSED LOOP</th>
<th>OPEN LOOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SΦCL(f)</td>
<td></td>
<td></td>
<td>SΦOL(f)</td>
</tr>
<tr>
<td>fL</td>
<td></td>
<td></td>
<td>Ni / f^2</td>
</tr>
<tr>
<td>f</td>
<td></td>
<td></td>
<td>f</td>
</tr>
</tbody>
</table>

TIME DOMAIN

<table>
<thead>
<tr>
<th>TRANSMIT CLOCK REFERENCED</th>
<th>SELF REFERENCED</th>
</tr>
</thead>
<tbody>
<tr>
<td>p(t)</td>
<td>p(t)</td>
</tr>
<tr>
<td>σx</td>
<td>σx</td>
</tr>
</tbody>
</table>

FREQUENCY DOMAIN

<table>
<thead>
<tr>
<th>PLL CLOSED LOOP</th>
<th>OPEN LOOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SΦCL(f)</td>
<td>SΦOL(f)</td>
</tr>
<tr>
<td>Ni / f^2</td>
<td></td>
</tr>
</tbody>
</table>

SELF REFERENCED

<table>
<thead>
<tr>
<th>σΔT(CL)(ΔT)</th>
<th>σΔT(OL)(ΔT)</th>
</tr>
</thead>
</table>

McNEILL: JITTER IN PHASE-LOCKED LOOPS
### Mathematical relationships preview

<table>
<thead>
<tr>
<th>PLL CLOSED LOOP</th>
<th>OPEN LOOP</th>
<th>TIME DOMAIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY DOMAIN</td>
<td></td>
<td>TRANSMIT CLOCK REFERENCED</td>
</tr>
<tr>
<td>$F \frac{N_1/f_L^2}{1 + (f/f_L)^2}$</td>
<td>$S_{\phi_L}(f) = \frac{N_1}{f^2}$</td>
<td>$\sigma_x = \frac{1}{f_o} \sqrt{\frac{N_1}{4\pi f_L}}$</td>
</tr>
<tr>
<td>$K^2 \frac{(f_o/f_L)^2}{1 + (f/f_L)^2}$</td>
<td>$N_1 = K^2 f_o^2$</td>
<td>$\sigma_x = K \sqrt{\frac{1}{4\pi f_L}}$</td>
</tr>
<tr>
<td>$\sigma_{\Delta T(CL)}(\Delta T)$</td>
<td>$\sqrt{2} \sigma_{\phi_O}(f)$</td>
<td>$\sigma_{\Delta T(OL)}(\Delta T) = K \sqrt{\Delta T}$</td>
</tr>
</tbody>
</table>
Benefits of time/frequency technique

- Can relate either open loop figure of merit ($\kappa$ or $N_1$) to closed loop jitter performance.
- Allows design to take place in most convenient domain.
- Simplifies design and simulation: need only consider open loop VCO.
- Allows stand-alone test of VCO contribution to jitter.
- Applies to any oscillator that fits $1/f^2$ model.

BUT...

- $\kappa$ and $N_1$ describe jitter performance of the entire oscillator: How to relate to design decisions on the level of the ring delay stage?
## Applications Overview

<table>
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<tr>
<th>Time Domain</th>
<th>Frequency Domain</th>
</tr>
</thead>
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<tr>
<td>Sonet / serial data communication</td>
<td>Wireless communication</td>
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<tr>
<td>High speed clock synthesis (multiply-by-N)</td>
<td>Oversampling ADC / digital audio</td>
</tr>
<tr>
<td>Clock distribution (“zero delay buffer”)</td>
<td></td>
</tr>
</tbody>
</table>
SONET Application

- Serial data transmission over fiber optic link

- Bit rates:
  - OC-3 155.52MHz
  - OC-12 622.08MHz
  - OC-48 2.488GHz
Clock Recovery with PLL

- Frequency detector aids initial acquisition
- Assume charge pump PD, typical loop filter
### SONET Standard Documents

- Available from Telcordia (formerly Bellcore)
- **GR-253-CORE**
  - Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria ($1,500)
- **GR-1244**
  - Clocks for the Synchronized Network: Common Generic Criteria ($85)
- **TR-NWT-000917**
  - SONET Regenerator (SONET RGTR) Equipment Generic Criteria ($110)

[Source for information in this section]
SONET Specifications

- Jitter Generation
- Jitter Transfer
- Jitter Peaking
- Jitter Tolerance
- Wander
- Time Interval Error
- Time Deviation / Time Variance
- Holdover
Jitter / Wander

• “Two sides of same coin”
• Jitter:
  – Phase error > 10Hz modulation
  – Defined in terms frequency content of modulation
  – Test in time or frequency domain
• Wander:
  – Phase error < 10Hz modulation
  – Defined over observation time > 0.1sec
  – Test with Time Interval Analyzer
<table>
<thead>
<tr>
<th>Jitter Generation</th>
</tr>
</thead>
<tbody>
<tr>
<td>• SONET Specification:</td>
</tr>
<tr>
<td>• rms output jitter $\leq 0.01$ unit interval (UI)</td>
</tr>
<tr>
<td>• Assumes jitter-free serial data input</td>
</tr>
<tr>
<td>• Test in time domain (TCLK referenced)</td>
</tr>
</tbody>
</table>
Jitter Tolerance

- **SONET Specification:**
  - Tolerate p-p jitter with equivalent 1dB BER penalty
  - Test with BER tester

### Frequency Table

<table>
<thead>
<tr>
<th>OC/STS Level</th>
<th>f0 (Hz)</th>
<th>f1 (Hz)</th>
<th>f2 (Hz)</th>
<th>f3 (kHz)</th>
<th>ft (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>48</td>
<td>10</td>
<td>600</td>
<td>6000</td>
<td>100</td>
<td>1000</td>
</tr>
<tr>
<td>24'</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>10</td>
<td>30</td>
<td>300</td>
<td>25</td>
<td>250</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>30</td>
<td>300</td>
<td>6.5</td>
<td>65</td>
</tr>
</tbody>
</table>

Jitter Transfer / Peaking

• SONET Specification:
  • Transfer function from input phase to output phase
  • Test with amplitude from jitter tolerance

TYPICAL TRANSFER FUNCTION

0 dB

P

c

Range

Acceptable

slope = -20 dB/decade

<table>
<thead>
<tr>
<th>OC/STS Level(^1,2)</th>
<th>fc (kHz)</th>
<th>P (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>48</td>
<td>2000</td>
<td>0.1</td>
</tr>
<tr>
<td>24(^3)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>500</td>
<td>0.1</td>
</tr>
<tr>
<td>3</td>
<td>225</td>
<td>0.1</td>
</tr>
</tbody>
</table>

3. Not specified in GR-253 or G.958.
• Jitter transfer critical in regenerator
• Any peaking will accumulate
Maximum Time Interval Error

- SONET Definition

![Diagram showing time delay and intervals](image-url)
<table>
<thead>
<tr>
<th>Time Deviation / Time Variance</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Standard deviation of Time Interval Error</td>
</tr>
<tr>
<td>– observed over a given time interval</td>
</tr>
<tr>
<td>• Time domain test</td>
</tr>
<tr>
<td>– Two sample standard deviation</td>
</tr>
<tr>
<td>• Test with</td>
</tr>
<tr>
<td>– CSA (short interval)</td>
</tr>
<tr>
<td>– Time interval analyzer (long interval)</td>
</tr>
</tbody>
</table>
## Holdover

- Maintain stable frequency with no transitions at input
- **Factors:**
  - Charge pump leakage
  - VCO stability
Recovery from Holdover

t₀ enter holdover  t₁ reference available  2t₁ reference valid
## SONET Application Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Detail</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jitter Generation</td>
<td>0.01 UI rms</td>
</tr>
<tr>
<td>Jitter Transfer</td>
<td>- Determines PLL loop bandwidth</td>
</tr>
<tr>
<td></td>
<td>- Jitter peaking critical in regenerator application</td>
</tr>
<tr>
<td>Holdover</td>
<td>- Maintain frequency in absence of input data</td>
</tr>
<tr>
<td></td>
<td>- Some wander allowed</td>
</tr>
<tr>
<td></td>
<td>- Limit phase transient in recovery from holdover</td>
</tr>
</tbody>
</table>
High Speed Clock Synthesis / Multiplication

- High speed digital clock distribution
  - Distribute low frequency clock
  - Use on-chip PLL to multiply to higher frequency
  - Jitter reduces timing margin

\[ \theta_o \div N \]

\[ \theta_i \]
“Zero delay buffer”

- Phase lock output clock to input
- Use on-chip PLL to generate clock

![Diagram of a phase-locked loop with a zero delay buffer](image-url)
Typical Specifications

- **Static phase**
  - Measure in time domain; input clock reference

- **Cycle-to-cycle jitter**
  - Measure in time domain; self referenced
  - \( \kappa \) model applied to one cycle of clock

- **Spread spectrum**
  - Intentionally add “jitter” to improve EMC
Spread spectrum

- Intentionally add “jitter” to improve EMC
- Modulate inside loop (usually VCO input)
- Reduces spectral peak: improves EMC
Oversampling ADC/DAC / Digital Audio

- Digital audio / oversampled data conversion
  - PLL used to generate multiple of fundamental sampling rate required for Σ-Δ ADC/DAC
  - Phase noise causes audible distortion
  - “Smearing” in convolution by non-impulse

- Test in frequency domain
Effect of Phase Noise

Ideal sampling clock (impulse):

Real sampling clock (with phase noise):

"Smearing" of frequency content in sampling (convolution)
<table>
<thead>
<tr>
<th>Wireless Communication</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Wireless communication</td>
</tr>
<tr>
<td>– PLL used in demodulation of RF signal</td>
</tr>
<tr>
<td>– Requires low phase noise LO</td>
</tr>
<tr>
<td>• Bluetooth</td>
</tr>
<tr>
<td>– Wireless personal device connectivity</td>
</tr>
<tr>
<td>• DECT</td>
</tr>
<tr>
<td>– Digital cordless telephone</td>
</tr>
<tr>
<td>• Test in frequency domain</td>
</tr>
</tbody>
</table>
## Typical Specifications

- **DECT**: 1.6GHz to 2.0 GHz
- **Phase noise:**
  - $-99\text{dBc/Hz @ 1.7MHz offset}$
  - $-117\text{ dBc/Hz @ 3.2 MHz offset}$
  - $-131\text{ dBc/Hz @ 4.7MHz offset}$
Example of DECT Phase Noise Specification

CARRIER POWER
+6 dBm

PHASE NOISE at 1.7MHz OFFSET (NORMALIZED TO CARRIER POWER)
-93dBm/Hz - (+6dBm) = -99dBc/Hz
("dBc" = "dB RELATIVE TO CARRIER")

PHASE NOISE POWER DENSITY
-93 dBm/Hz
Overview: Practical Measurement Techniques

- **Time Domain**
  - Tektronix CSA803 / 11801
  - Other techniques (Time Interval Analyzer)
- **Frequency Domain**
  - Spectrum Analyzer
  - Other techniques (Phase Noise Analyzer)
- **Circuit-level issues**
  - 50Ω interface
  - Signal Integrity
  - Common Pitfalls
Time domain

- Tektronix CSA803/11801
- Equivalent time sampling scope
- 1psec/div time domain resolution
Equipment Requirements

- Minimum requirements to achieve desired accuracy
- "Jitter floor"
  - Uncertainty of CSA time base depends on delay
  - Assume independent: adds in rms fashion
    \[ \sigma_{TOTAL} = \sqrt{\sigma_{CSA}^2 + \sigma_{SIGNAL}^2} \]
  - Error \( \approx 10\% \) when \( \sigma_{CSA} = \frac{1}{2} \sigma_{SIGNAL} \)
CSA “Jitter Floor”

Measured Tektronix 11801C
"Jitter Floor"

rms Jitter (psec)
Example: Show jitter floor next to all data plotted

- Software controls CSA over HPIB
- Also show $\kappa \sqrt{\Delta T}$ plot
Triggering

• Separate trigger input
  – Can’t trigger off “scope display”

Solutions:

Differential output buffer

Power splitter

ECL (e.g. 10H124)

(6 dB LOSS)
Triggering: Duty cycle distortion / jitter

- More common with single-ended systems
- Usually not important for timing (use good edge)
- Very important for phase noise!
  (spectrum analyzer “sees” both edges)
- Choose correct (same) edge for all measurements
- Increase in measured jitter if “wrong” edges used

CLK
CLK
"GOOD EDGE"
"BAD EDGE"
CLK
Problems: Minimum Delay

- Minimum delay from trigger to first sample: \(~ 30\text{nsec}\)
- Use cable delay line
- Watch out for "mechanical jitter"
  \((1\text{psec} = 0.3\text{mm change in electrical length})\)
<table>
<thead>
<tr>
<th>Other time domain methods</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TIA (Time Interval Analyzer)</strong></td>
</tr>
<tr>
<td>• <strong>Advantage</strong></td>
</tr>
<tr>
<td>– More accurate at long delays</td>
</tr>
<tr>
<td>• <strong>Disadvantage</strong></td>
</tr>
<tr>
<td>– Not a sampling scope:</td>
</tr>
<tr>
<td>• no picture of waveform</td>
</tr>
<tr>
<td>• no indication of reflections / signal integrity problems</td>
</tr>
<tr>
<td>Frequency domain</td>
</tr>
<tr>
<td>------------------</td>
</tr>
</tbody>
</table>

- **Spectrum Analyzer**
  - General purpose frequency domain instrument
  - Example: HP8560E used for following plots

- **Phase Noise Analyzer**
  - Optimized for phase noise measurements
  - HP3048

- **Test Options**
  - Phase noise plot
  - Phase noise at a specified offset frequency
  - (“Spot Frequency”)
Spectrum Analyzer (HP8560E)

Source: Hewlett-Packard Application Note AN-150
Phase Noise Measurement

- **HP85671A Phase noise “plug-in”**
  - Measures noise power density at offset frequencies near carrier peak

- **Equipment requirements**
  - Spectrum analyzer phase noise floor depends on frequency
  - Test with HP8648D low-phase-noise signal source
HP8560E Phase Noise Floor: 155 MHz

10 dB/RL -50 dBc/Hz

SPOT FRQ = 100.0 kHz

100 Hz FROM 155.5 MHz CARRIER 10 MHz

-120.00 dBc/Hz
HP8560E Phase Noise Floor: 622 MHz
HP8560E Phase Noise Floor: 2488 MHz
### Noise measurement cautions

- **Common pitfalls to watch out for**
  - BW filter shape
  - Amplitude noise / phase noise ambiguity
  - Noise units problem (older spectrum analyzers)
Incorrect Resolution Bandwidth

- Phase noise peak narrower than RBW filter
- Plot shows shape of RBW bandpass filter (not phase noise!)
Correct Resolution Bandwidth

**INCORRECT**
- RBW filter too wide

**CORRECT**
- RBW filter narrower than phase noise
- Note loooong sweep time!
Amplitude noise / phase noise ambiguity

- Spectrum analyzer responds to magnitude
- AM, PM spectra indistinguishable
- Solution: use limiter:

\[ \text{ECL GATE} \]
\[ \text{(OR COMPARATOR IF Vin SMALL)} \]
Noise units problem (some spectrum analyzers)

- Spectrum analyzer uses envelope detector to determine magnitude of frequency component
- Sinusoid vs. Gaussian noise: Detector response different!
- Units:
  - Carrier: power (dBm) in (ideal) impulse
  - Noise: power density (dBm/Hz) per unit bandwidth
  - Phase noise: dBc/Hz (normalize to carrier power)
- May need “fudge factor” to account for envelope detector on some spectrum analyzers
  - HP Application Note AN-150
Other time domain techniques: Phase Noise Analyzer

- HP E5500 series ~ $40,000+ (replaces discontinued HP3048)
- Generally better than required for integrated VCOs
Interfacing to 50Ω input

• ECL/PECL coupling network:

- ECL/PECL coupling network:
  - ECL (e.g. 10H116)
  - $v_{CC} = +5V$
  - 100Ω
  - 100Ω
  - SMA or SMB
  - 1000pF
  - 1000pF
  - (CERAMIC NPO)
  - (ALL R, C SURFACE MOUNT)
CMOS-ECL: Options for interfacing to 50Ω input

1) Use CMOS/TTL-to-ECL/PECL translator with 50Ω coupling network

2) Step-down RF transformer:

- Select based on minimum frequency
- Select based on route of CMOS driver
- Current drive requirement easier by $N^2$
- Caution: transformer bandwidth
Signal Integrity

• For evaluation boards, usual suspects:
  – Ground plane
  – Transmission line approach
  – Moderately well controlled impedance
    • Don’t need super-expensive PCB (622MHz)
  – SMA or SMB (or other RF connector)
  – SM components
  – Identical differential paths
Test Issues

• Observing nodes
• Testing multiple PLLs
• Self-test issues
• Choice of test/measurement
  – Time vs. frequency
  – Open loop vs. closed loop
• “Shortcuts” using measurement relationships
  – Time domain
  – Frequency domain
• Evaluation (pass/fail) vs diagnostic
Observing nodes

- Effects of bringing out PLL signal(s) to external pin(s)
  - VCO control voltage
  - VCO output
VCO control input

- **Advantage**
  - Measure VCO V-f characteristic
  - Close loop, lock to different f, measure $V_{\text{CTL}}$
  - Could force $V_{\text{CTL}}$ open loop, measure f (harder)

- **Indirect method**
  - Off-chip loop filter capacitor
  - (assumes negligible IR drop on $R_z$)

- **Disadvantage**
  - Noise coupling path to (sensitive) $V_{\text{CTL}}$ node
<table>
<thead>
<tr>
<th>VCO output</th>
</tr>
</thead>
<tbody>
<tr>
<td>• At-frequency testing</td>
</tr>
<tr>
<td>• When needed, when is it not required</td>
</tr>
<tr>
<td>• Problem: driving GHz to off-chip pins</td>
</tr>
</tbody>
</table>
Divide Down VCO Output

- Possibility: bring out divided-by-M version
  - Register to avoid pattern jitter
- Time domain:
  - Same jitter $\kappa$
- Frequency domain:
  - Phase noise power divided by factor $M^2$
- Don't divide by too much:
  - Might be better than spectrum analyzer!
Multiple PLL testing

- Multiplex to single output pin
- Watch out for crosstalk paths

- Multiplexer
  - Disable other mux inputs

- Other paths (e.g. substrate)
  - Switch off everything else if possible

- Jitter through mux path usually not too bad
  - Doesn't accumulate
Self-Test Issues

- Open loop test vs. close loop test
- Frequency
- Phase noise
- Jitter
- Choice of conditions
Open vs. closed

- Open better / simpler
- No need for precise source (but do need low noise "zero" input to VCO)
- No need to wait for acquisition
- Open loop parameters can be related to closed loop performance
<table>
<thead>
<tr>
<th>Time, frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Depends on application/specification</td>
</tr>
</tbody>
</table>
Frequency self-test

• Open loop - on-chip counter to count cycles during externally set time window

\[ f = \frac{N}{T_G} \]
Center Frequency self-test

- Center Frequency: short VCO input

![Diagram of a phase-locked loop with a VCO, loop filter, charge pump, and test point.](image)
Tuning range self-test

• Max - min range
• Min max frequency by disabling PD or ramping charge pump to +/- rails
• Saturate VCO input +/-
• Indication of ability to cover tuning range
• Advantage: can be done “digitally” (no need for good quality analog shorting switch)
Time Domain Shortcuts

- Could compile full $\sigma$ vs. delay plot
- Establishes confidence in $\kappa$ model
- Or shortcut: just check at single delay

\[ \sigma = \kappa \sqrt{\Delta T} \]

\[ \sigma_x = \kappa \sqrt{\frac{1}{4\pi f_L}} \]

\[ \tau_L = \frac{1}{2\pi f_L} \]

“SHORTCUT” FROM t-f RELATIONSHIPS

CLOSED LOOP JITTER

LOOP BANDWIDTH

TIME CONSTANT
### Frequency Domain Shortcuts

- Could compile full phase noise plot
- Establishes confidence in $1/f^2$ model
- Or shortcut: just check at specified offset
Phase noise self-test

- Could measure phase noise with VCO input railed (VCO output at $f_{\text{min}}$ or $f_{\text{max}}$)
- If VCO has unusual characteristic, may want to short out in midscale

![Diagram showing phase noise self-test]
### Choice of Measurement

- **Evaluation (pass/fail) vs. diagnostic**
- **Pass/fail**
  - Single ("shortcut") measurements
- **Diagnostic**
  - Full plots
  - Structure shows information
<table>
<thead>
<tr>
<th>Crosstalk/Coupling Diagnostic</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Crosstalk / interference issues</td>
</tr>
<tr>
<td>• Theory predicts what closed loop jitter / phase noise should be based on open loop</td>
</tr>
<tr>
<td>• Close loop, run other circuitry</td>
</tr>
<tr>
<td>• Look for artifacts</td>
</tr>
<tr>
<td>– Frequency domain: spurs etc.</td>
</tr>
<tr>
<td>– Time domain: increased jitter</td>
</tr>
</tbody>
</table>
Crosstalk/Coupling Diagnostic Example

- On-chip coupling of digital noise from phase detector
- Jitter higher at low delays when loop closed

\[ \kappa = 6.14 \times 10^{-8} \, \sqrt{\text{s}} \]
Overview: Design Techniques

- VCO Design using $\kappa$ figure-of-merit (time domain)
- Noise models for CMOS ring VCOs
- System level design issues
  - Loop bandwidth
  - Single-ended vs. differential
  - Delay Lock Loop (DLL)
- Other VCO design techniques
  - Transient noise source simulation
  - LC oscillator
  - VCO design in frequency domain
VCO Design Using $\kappa$ Parameter

Open loop:

$\sigma$ proportional to square root of $\Delta T$

$$\sigma_{\Delta T(OL)}(\Delta T) \approx K \sqrt{\Delta T}$$

- Fit to $\kappa = 6.14E-08 \sqrt{s}$
- Measured jitter

![Graph showing rms jitter vs. delay $\Delta T$]
Benefits of Designing With $\kappa$

- Can relate either open loop figure of merit ($\kappa$ or $N_1$) to closed loop jitter performance.
- Allows design to take place in most convenient domain
- Simplifies design and simulation: need only consider open loop VCO
- Allows stand-alone test of VCO contribution to jitter.
- Applies to any oscillator that fits $1/f^2$ model

BUT...

- $\kappa$ and $N_1$ describe jitter performance of the entire oscillator: How to relate to design decisions on the level of the ring delay stage?
Effect of Length of Ring

- Rings of lengths 3, 4, 5, 7, and 9 stages were fabricated
- All delay stages identical

What effect does the length of the ring have on jitter?
Schematic of Ring Stage for Experiments
Results: Ring Length Not A Factor!

<table>
<thead>
<tr>
<th>RING STAGES</th>
<th>$\kappa$ [E-08s]</th>
<th>$f_0$ [MHz]</th>
<th>$t_d$ [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>4.17</td>
<td>170.1</td>
<td>980</td>
</tr>
<tr>
<td>4</td>
<td>3.56</td>
<td>164.1</td>
<td>762</td>
</tr>
<tr>
<td>5</td>
<td>3.78</td>
<td>102.7</td>
<td>974</td>
</tr>
<tr>
<td>7</td>
<td>3.77</td>
<td>71.9</td>
<td>993</td>
</tr>
<tr>
<td>9</td>
<td>3.94</td>
<td>56.8</td>
<td>978</td>
</tr>
</tbody>
</table>

- Jitter depends only on number of gates traversed, not number of oscillator periods:
- Length of ring is not a factor!
- Only need to consider $\kappa$ of individual gate to know jitter performance of ring
Ring length experiment: Handwaving explanation

- Example: two rings: 3-stage and 5-stage
- 10nsec delay per stage (all stages identical)
- What is jitter after 150nsec delay?
Ring length experiment: Handwaving explanation

- Jitter will be the same for each ring
- In both cases, edge has traversed 15 gate delays
- Jitter errors added in each delay are independent
- Note: edge has not traversed same number of oscillator periods
  - When analyzing jitter in ring oscillators, the gate delay is the fundamental unit of time, not the oscillator period

![Diagram showing ring length experiment with A B C D E and A' B' C']
<table>
<thead>
<tr>
<th>Meaning of ring length experiment</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Can design ring from single gate</td>
</tr>
<tr>
<td>• Determine $\kappa$ for one gate</td>
</tr>
<tr>
<td>• Within gate, find $\kappa$ for each noise source</td>
</tr>
</tbody>
</table>
## Benefits of Designing With $\kappa$

- Can predict system level closed loop jitter as a function of circuit level parameters (resistor values, currents, etc.)
- Quick estimate of achievable jitter as a function of fundamental parameters
  - Power dissipation
  - Signal amplitude
- Identifies major source(s) of jitter
- $\kappa$ independent of:
  - Number of stages in ring $N$
  - Load capacitance $C$
- Allows designer freedom to choose $N$, $C$ to set center frequency without affecting jitter
  - Usually: few stages (3 or 4), maximize power for lowest jitter
### Design Strategy

<table>
<thead>
<tr>
<th>System level:</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Determine PLL loop bandwidth</td>
</tr>
<tr>
<td>- Determine (system-level) $\kappa$ for required performance</td>
</tr>
<tr>
<td>VCO level: determine</td>
</tr>
<tr>
<td>- Center frequency</td>
</tr>
<tr>
<td>- Number of stages (usually 3 or 4)</td>
</tr>
<tr>
<td>- Individual gate delay</td>
</tr>
<tr>
<td>Gate level:</td>
</tr>
<tr>
<td>- System-level $\kappa$ also applies to gate</td>
</tr>
<tr>
<td>- Design individual gate stage to meet $\kappa$</td>
</tr>
<tr>
<td>- Depends on circuit architecture</td>
</tr>
</tbody>
</table>
Gate level design

• Assumptions
• Types of ring delay stages
  – Bipolar ECL (differential)
  – CMOS ECL (differential)
  – CMOS inverter (single-ended)
• $\kappa$ expressions for noise sources
• Experimental results
## Assumptions

- **Dominated by white noise**
  - $1/f$ noise negligible
  - Inside PLL bandwidth
- **Noise sources independent**
  - Add in rss fashion
- **“Dominant pole”**
  - Only one major delay mechanism
  - Load capacitance
Bipolar ECL Gate Level Sources of Jitter

Differential pair delay stage

Delay stage with noise sources
Handling Multiple Noise Sources

- Each source independent
- Contributions will add in rms fashion
- Find $\kappa$ due to each noise source
Collector Resistance Noise Model

\[ K_{RC} \approx (1.699) \sqrt{\frac{kT}{I_{EE}R_C}} \]
Collector R noise result

Voltage standard deviation (amplitude noise):

\[ \sigma_V = \sqrt{\frac{2kT}{C_C}} \]

Slope at zero crossing:

\[ S = \frac{dV}{dt} = \frac{I_{EE}}{C_C} \]

Time standard deviation (jitter):

\[ \frac{\sigma_V}{\sigma_t} = \frac{dV}{dt} \quad \Rightarrow \quad \sigma_t = \frac{\sigma_V}{dV/dt} = \sqrt{\frac{2kTC_C}{I_{EE}^2}} \]
\( \kappa \) for collector R noise result

**Gate delay:**

\[
T_d = \ln(2) R_C C_C
\]

**Time standard deviation (jitter):**

\[
\sigma_t = \sqrt{\frac{2kT C_C}{I_{EE}^2}}
\]

**Definition of \( \kappa \):**

\[
\kappa = \frac{JITTER}{\sqrt{DELAY}} = \frac{\sigma_t}{T_d}
\]

\[
\kappa = \sqrt{\frac{2}{\ln(2)}} \sqrt{\frac{kT}{I_{EE}^2 R_C}}
\]

**Key:** DC power dissipation in \( R_C \)
Tail current source noise model

General form of $\kappa$ expression:

$$\kappa = \frac{1}{2 \sqrt{\ln(2)}} \frac{i_n}{I_{EE}}$$
## Tail current noise result

**Noise dominated by thermal noise in degeneration resistor $R_E$:**

\[
\kappa = \frac{1}{\sqrt{\ln(2)}} \sqrt{\frac{kT}{I_{EE}^2 R_E}}
\]

**Similar to collector resistor result**

**Key: DC power dissipation in degeneration resistor $R_E$**

**Noise dominated by shot noise of bias current $I_{EE}$:**

\[
\kappa = \frac{1}{\sqrt{2 \ln(2)}} \sqrt{\frac{q_e}{I_{EE}}}
\]

![Graph showing tail current noise result with Vc2, Vc1, Vn2(t), Vn1(t), and Vc2 - Vc1 over time (t).](image)
Switched input noise model

- Bipolar differential pair
- Convenient analytical expression for transconductance $g_m$
\[ \kappa = \frac{1}{\sqrt{6 \ln(2)}} e_n \sqrt{\frac{g_m}{I_{EE}^2 R_C}} \]

Keys:
- DC power dissipation in degeneration resistor \( R_E \)
- Peak transconductance \( g_m \)
- Total input referred noise density \( e_n \)
Validation: $\kappa$ vs. Tail Current $I_{EE}$

Fig. 4.20. $\kappa$ vs. tail current $I_{EE}$. $\kappa \left[ E^{-08}\sqrt{sec} \right]$
\( \kappa \) due to input-referred noise in VCO control path

\[
\kappa = \frac{1}{\sqrt{2}} \frac{K_O}{\omega_O} e_{n(VCO)}
\]

- Applies to any VCO dominated by input white noise (or equivalent)
- Parameters:
  \( K_O \) VCO control constant
  \( \omega_O \) VCO center frequency
  \( e_{n(VCO)} \) Noise in VCO control path referred to VCO input
- Use compatible units for \( K_O, \omega_O \):
  \( \frac{Hz}{V} \) \( OR \) \( \frac{rad}{(V \cdot sec)} \) \( OR \) \( \frac{rad}{sec} \)
### Bipolar Differential Pair $\kappa$ Expression Summary

<table>
<thead>
<tr>
<th>Expression</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\kappa = \frac{2}{\ln(2)} \sqrt{\frac{kT}{I_{EE}^2 R_C}}$</td>
<td>Differential pair collector load resistance</td>
</tr>
<tr>
<td>$\kappa = \frac{1}{\ln(2)} \sqrt{\frac{kT}{I_{EE}^2 R_E}}$</td>
<td>Tail current (thermal dominated)</td>
</tr>
<tr>
<td>$\kappa = \frac{1}{\ln(2)} \sqrt{\frac{kT}{q I_{EE}}} e_n$</td>
<td>Tail current (shot noise dominated)</td>
</tr>
<tr>
<td>$\kappa = \frac{1}{\sqrt{6 \ln(2)}} e_n \sqrt{\frac{g_m}{I_{EE}^2 R_C}}$</td>
<td>Differential pair input referred noise</td>
</tr>
<tr>
<td>$\kappa = \frac{1}{\sqrt{2} \omega_O} e_n(VCO)$</td>
<td>Input referred noise of VCO control path</td>
</tr>
</tbody>
</table>

Dominant contributor depends on details of VCO design.
Intuitive meaning of \( K \) expressions

- Time domain figure of merit \( K \):
  - has dimensions of square root (time)
  - quantifies gate's ability to measure time accurately

- All equations for \( K \) take form:
  \[
  \sqrt{\text{UNCERTAINTY IN QUANTITY}} / \sqrt{\text{QUANTITY FLOW RATE}}
  \]

- \( K \) from thermal noise in collector load resistor \( R_C \)
  \[
  K_{RC} \approx (1.699) \sqrt{\frac{kT}{I_{EE}^2 R_C}} \quad \sqrt{\frac{\text{joule}}{\text{joule/sec}}}
  \]

- \( K \) from shot noise in tail current \( I_{EE} \)
  \[
  K_{I_{EE}} \approx (0.849) \sqrt{\frac{q}{I_{EE}}} \quad \sqrt{\frac{\text{coul}}{\text{coul/sec}}}
  \]
Differential CMOS Noise Sources

Differential pair delay stage

Delay stage with noise sources
κ expressions: load resistance, tail current

Differential pair drain load resistance

\[
\kappa = \sqrt{\frac{2}{\ln(2)}} \sqrt{\frac{kT}{I_{SS}^2 R_L}}
\]

Tail current

\[
\kappa = \frac{1}{2\sqrt{\ln(2)}} \frac{i_n}{I_{SS}}
\]

Analogous to bipolar differential pair expressions

Switching action of differential pair similar in both cases
\( \kappa \) expression: switched input noise model

- MOS differential pair
- No nice analytical expression for transconductance \( g_m \)
- Use approximation
\[ \kappa \text{ expression: switched input noise} \]

Approximating transconductance \( g_m \) as shown:

\[ \kappa = \kappa \text{ due to input referred noise } e_n : \]

\[ \kappa = \frac{1}{2\sqrt{\ln(2)}} e_n \sqrt{\frac{g_m}{I_{SS}^2 R_L}} \]

Again, analogous to bipolar differential pair expression.
### MOS Differential Pair $\kappa$ Expression Summary

<table>
<thead>
<tr>
<th>Term</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential pair drain load resistance</td>
<td>$\kappa = \sqrt{\frac{2}{\ln(2)}} \sqrt{\frac{kT}{I_{SS}^2 R_L}}$</td>
</tr>
<tr>
<td>Tail current</td>
<td>$\kappa = \frac{1}{2\sqrt{\ln(2)}} \frac{i_n}{I_{SS}}$</td>
</tr>
<tr>
<td>Differential pair input referred noise</td>
<td>$\kappa = \frac{1}{2\sqrt{\ln(2)}} e_n \sqrt{\frac{g_m}{I_{SS}^2 R_L}}$</td>
</tr>
<tr>
<td>Input referred noise of VCO control path</td>
<td>$\kappa = \frac{1}{\sqrt{2}} \frac{K_O}{\omega O} e_n(VCO)$</td>
</tr>
</tbody>
</table>

Does not include short channel effects!
$\lambda$ Expressions: Implications for Design

- For lower jitter, need lower $\lambda$
- Denominator of all gate-level $\lambda$ expressions have
  - current $I$
  - power dissipation $I^2R$
  - voltage signal swing $IR$
  $\Rightarrow$ For lower jitter, need to increase current, power, swing
- Implication:
  $\Rightarrow$ As supply voltages, allowable power dissipation decrease, low jitter becomes harder to achieve
Single-ended CMOS Ring Oscillator

- Research underway (NSF CAREER grant)
- Test chip evaluation to be completed Dec 1999
- Preliminary results indicate similar tradeoffs
  - power dissipation, voltage swing vs. jitter
- Caution: single-ended approach more prone to supply, substrate noise coupling
  - increases apparent jitter above theoretical limit set by fundamental noise mechanisms expressed in $\kappa$ relationships
Example of $\kappa$ design:

- 155.52MHz SONET jitter specification
- Goal: from system-level specification, estimate required gate-level parameters such as voltage swing, power dissipation, bias current, etc.
- Required jitter $\sigma_x = 0.01$UI
- One UI = 1 / 155MHz = 6.43 nsec
- $0.01$UI = 6.43 nsec / 100 = 64.3 psec
- 2X safety margin: try for $\sigma_x = 32$ psec
Example of $\kappa$ design:

- System-level $\sigma_x$ related to gate-level $\kappa$ by time-frequency relationships:
  \[
  \sigma_x = \kappa \sqrt{\frac{1}{4\pi f_L}} \quad \Rightarrow \quad \kappa = \sigma_x \sqrt{4\pi f_L}
  \]

- Loop bandwidth $f_L = 200$ kHz (from SONET spec)
  \[
  \kappa = (32\, p\, sec) \sqrt{4\pi (200\, kHz)} \quad \Rightarrow \quad \kappa = 5.1E-8 \, \sqrt{\text{sec}}
  \]

- Estimate: apportion $\kappa$ equally from four sources
  $\kappa = 2.5E-8 \, \sqrt{\text{sec}}$ for each source
Example of κ design: Load power dissipation

- **κ expression for load resistance**
  \[ \kappa = \sqrt{\frac{2}{\ln(2)}} \sqrt{\frac{kT}{I_{SS}^2 R_L}} \]

- At T=300K, estimated power dissipation required in load element is
  \[ 2.5E-8 = \sqrt{\frac{2}{\ln(2)}} \sqrt{\frac{(4.0E-21)}{I_{SS}^2 R_L}} \quad \Rightarrow \quad I_{SS}^2 R_L = 18.3\mu W \]

- If maximum allowable voltage swing is limited (for example, to I_{SS}R_L = 0.3V), then required bias current is
  \[ 18.3 \mu W / 0.3 V = 61 \mu A \]
Example of $\kappa$ design:

- Similar estimates can be calculated for other contributors:
  - tail current noise
  - input referred noise of differential pair
  - noise in VCO control input path
- Allocations to total $\kappa$ can be revised
  - refine original “all contribute equally” apportionment
- Identify dominant contributor
  - where to push for maximum jitter benefit
Example of K design (AD806)

- Applications and performance requirements
- Development of basic ring VCO
- Shortcomings of basic VCO
  - Design improvements
  - Experimental results
- Summary
AD80X clock recovery: design goals

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>GOAL</th>
<th>MEASURED RESULT</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CENTER FREQUENCY $f_0$</td>
<td>155.52 MHz</td>
<td>155.5 MHz (trim)</td>
<td></td>
</tr>
<tr>
<td>TUNING RANGE</td>
<td>$\pm 10%$</td>
<td>$\pm 10%$</td>
<td></td>
</tr>
<tr>
<td>JITTER</td>
<td>60 ps rms 0.95 % UI</td>
<td>30 ps rms 0.5 % UI</td>
<td>Should also be insensitive to supply noise</td>
</tr>
<tr>
<td>LINEARITY</td>
<td>$\pm 5%$</td>
<td>$\pm 1%$</td>
<td>Affects closed loop parameters</td>
</tr>
<tr>
<td>TEMPERATURE DRIFT OF $f_0$</td>
<td>$\pm 10%$</td>
<td>$\pm 5%$</td>
<td>Stay within VCO tuning range over $T$</td>
</tr>
<tr>
<td>DUTY CYCLE</td>
<td>50 % $\pm 1%$</td>
<td>50 % $\pm 1%$</td>
<td>Important for phase detector</td>
</tr>
<tr>
<td>QUADRATURE</td>
<td>$90^\circ \pm 10^\circ$</td>
<td>---</td>
<td>For frequency detector; not critical</td>
</tr>
<tr>
<td>TOTAL PLL POWER (5V supply)</td>
<td>140 mA 700 mW</td>
<td>25 mA 125 mW</td>
<td>Low capacitance of DI process (XFCB)</td>
</tr>
</tbody>
</table>
Basic design

- Inherent 50% duty cycle
- Quadrature to the extent that stage delays are matched
- Control frequency by controlling stage delay

- Interpolation fraction $x$ controlled by differential $V_{CTL(diff)}$
- Avoid common mode influence
Basic VCO design

Requirements met:

- Low duty cycle distortion
- Quadrature
- Low power

Shortcomings:

- Control nonlinear
- Temperature drift
- Jitter from supply
Nonlinearity fix

- Delay interpolation: Linear in time $T$
- Frequency $f = 1/T$: inherently nonlinear V-to-f
- Simulated linearity error: $\pm 4\%$

![Graph showing frequency versus voltage control signal (VCTL(diff))](image)

- **FREQUENCY**
  - UNCOMPENSATED
  - WITH COMPENSATING NONLINEARITY

- **VCTL(diff)**
  - $-0.2V$
  - $+0.0V$
  - $+0.2V$
Nonlinearity Fix

- Translinear cell with emitter area unbalance $\lambda:1$ (CMOS-able)
- Well controlled compensating nonlinearity

Measured linearity

[Graph showing the relationship between VCO input voltage and output frequency with linear error percentage]
<table>
<thead>
<tr>
<th>Overview: other VCO design techniques</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Design / simulation (transient noise)</td>
</tr>
<tr>
<td>• System level design issues</td>
</tr>
<tr>
<td>• Other types of integrable VCOs</td>
</tr>
<tr>
<td>• Different design methodologies</td>
</tr>
<tr>
<td>• Stability / Loop Bandwidth Considerations</td>
</tr>
</tbody>
</table>
**Transient Noise Simulation**

- Transient simulation required for realistic modeling of noise effects in nonlinear circuit
- Picosecond time step + transient simulation + multiple gate VCO + large PLL = Long simulation time? NO!
- Only need to simulate one gate delay
- Find $\sigma_t$ (sample standard deviation of delays)
- $\sigma_t/\sqrt{\text{delay}} = \kappa$ (time domain figure-of-merit)
- Use relationships for system-level performance
Transient noise source design/simulation

- Monte Carlo ≈ 100 simulations
- Use mean, standard deviations of simulated delays $T_{d1}, T_{d2}, \ldots$
Simulation: Transient Noise source

Pulsed sample-and-hold waveform for transient noise simulation.

Autocorrelation of pulsed sample-and-hold waveform
Single-sided PSD of PSH waveform

Choose $T \approx 1/10$ of shortest time constant

$2 \sigma_v^2 T$
Specifying Transient Noise Source

• Choose $T \approx 1/10$ of shortest time constant
• Choose $\sigma_v$ for desired noise density $e_n$

\[ \sigma_v = \frac{e_n}{\sqrt{2T}} \]

• Or choose $\sigma_i$ for current noise density $i_n$

\[ \sigma_i = \frac{i_n}{\sqrt{2T}} \]
System level design issues

- Reducing $\kappa$ improves gate-level influences on jitter
- What design options are available at the system level?
  - VCO level
    - Single-Ended vs. Differential
  - PLL level
    - Choice of Loop Bandwidth
  - Architecture level
    - Delay Lock Loop (DLL)
VCO design issues: Differential vs. single-ended

• Differential signal in VCO
  – Advantage: much better immunity to coupling of common mode noise (supply, substrate, crosstalk from digital signal lines)
  – Disadvantage: signal swing in differential pair usually limited to be much less than supply rails
    • κ expressions all indicate lower jitter with larger signal swing
• Single-ended signal in VCO
  – Advantage: allows larger signal swing, potentially lower jitter.
    BUT:
  – Disadvantage: probably won’t realize low theoretical jitter, since single-ended signal is much more susceptible to noise

⇒ Differential signal safer choice in “real-world” mixed signal chip
  • Corollary: maintain signal swing as large as possible (beware of VCO tuning methods that change signal amplitude)
System design issues: Loop Bandwidth

- Time-frequency relationships indicate that jitter (due to VCO phase noise) can be reduced by increasing the loop bandwidth $f_L$:

\[
\sigma_x = \kappa \sqrt{\frac{1}{4\pi f_L}}
\]

- Problems:
  - Often, no choice! Loop bandwidth determined by something else (e.g. SONET spec).
  - Pattern jitter if loop bandwidth is too large relative to frequency at phase detector output.
Pattern jitter example: synthesizer application

- Subtlety: Loop filter actually has two functions
  - Sets loop bandwidth (system-level controls analysis)
  - Also acts as a lowpass filter to “smooth” pulses at output of phase detector

![Phase-Locked Loop Diagram]

**Diagram Notes**

- IN -> PHASE DETECTOR
- PDOOUT -> LOOP FILTER
- OUT/N -> VCO
- VCTRL -> OUT
- +N -> OUT/N
Pattern jitter example: synthesizer application

- Subtlety: Loop filter actually has two functions
  - Sets loop bandwidth (system-level controls analysis)
  - Also acts as a lowpass filter to “smooth” pulses at output of phase detector

Long loop filter $\tau$ (narrow loop bandwidth) smooths PDOUT pulses at VCTL input

Loop filter $\tau$ too short (Loop bandwidth too wide)
System design issues: Loop Bandwidth Result

- Loop bandwidth $f_L$ usually can be no larger than a few percent of signal frequency at output of phase detector.

- If loop bandwidth is too high, pulses at phase detector output are not sufficiently smoothed at VCO control input.
  \[\Rightarrow\] Result of too-high $f_L$ is pattern jitter at VCO output.
System-Level Design: Delay Lock Loop

- Phase Lock Loop (PLL)
  - Synchronizes clock by generating a new clock with a VCO, then using phase detector in PLL to line up clock phases
- Delay Lock Loop (DLL)
  - Synchronizes clock using an adjustable delay to “slide” phase of existing clock in time.
  - Does not use a VCO to generate a clock
<table>
<thead>
<tr>
<th>DLL Advantages / Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Advantages</strong></td>
</tr>
<tr>
<td>– No jitter accumulations as in VCO</td>
</tr>
<tr>
<td>– Loop easier to stabilize</td>
</tr>
<tr>
<td><strong>Disadvantages</strong></td>
</tr>
<tr>
<td>– No output if input goes away (no &quot;holdover&quot;)</td>
</tr>
<tr>
<td>– Can't improve jitter of noisy source</td>
</tr>
<tr>
<td>– Difficult frequency multiplication</td>
</tr>
</tbody>
</table>
System-Level Design: Delay Lock Loop

• Consider DLL for some applications (e.g. clock synchronization at known clock frequency with low jitter)

• References:
<table>
<thead>
<tr>
<th>Jitter of Integrable VCOs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>• Ring</strong></td>
</tr>
<tr>
<td>– Empirical results show good jitter</td>
</tr>
<tr>
<td>– $\kappa$ expressions allow design for required performance</td>
</tr>
<tr>
<td><strong>• LC resonant</strong></td>
</tr>
<tr>
<td>– Known to have best jitter performance</td>
</tr>
<tr>
<td>– Small on-chip $L$ restricts frequency to $\geq 1 - 10$ GHz</td>
</tr>
<tr>
<td><strong>• Multivibrator</strong></td>
</tr>
<tr>
<td>– Known to have poor jitter performance</td>
</tr>
</tbody>
</table>
LC integrated VCO

• Bond wire inductance
  – Small L --> f ~ 10GHz

• Spiral inductor
  – Moderate L --> f ~ 1 GHz

• Problem:
  – Low Q due to substrate losses for L, C
  – Improve Q → improve phase noise
<table>
<thead>
<tr>
<th>Low Q solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Methods of improving LC resonator Q to improve phase noise</td>
</tr>
<tr>
<td>– Breaks in substrate</td>
</tr>
<tr>
<td>• Reduce eddy currents</td>
</tr>
<tr>
<td>– SOI</td>
</tr>
<tr>
<td>• Very high substrate resistance</td>
</tr>
<tr>
<td>– MEMS</td>
</tr>
<tr>
<td>• Etching away substrate</td>
</tr>
<tr>
<td>• Dec and Suyama, a 1.9GHz Micromachined-based Low-Phase-Noise CMOS VCO, ISSCC Digest of Technical Papers, Feb. 1999, pp. 80-81</td>
</tr>
</tbody>
</table>
Other design methodologies

• References for frequency domain (phase noise oriented) design methodologies:
Stability / Loop Bandwidth Considerations

• Typical synthesizer PLL application:

Loop filter transfer function (assume $C_1 \ll C_2$)

$$F(s) = \frac{1 + sR_ZC_2}{sC_2(1 + sR_ZC_1)}$$

For stability analysis, break PLL loop and find loop gain (loop transmission) $T(s)$

$$T(s) = \frac{I_{CP}K_{VCO}}{2\pi N} \frac{1 + sR_ZC_2}{s^2C_2(1 + sR_ZC_1)}$$
Loop transmission has: two poles at the origin, a zero (lead compensation) from $R_Z$, and a higher order pole from $C_2$.

For PLL to be stable (adequate phase margin), it is necessary that

$$
\frac{1}{R_Z C_2} \ll \omega_t \ll \frac{1}{R_Z C_1}
$$

where $\omega_t$ will be the loop bandwidth

Given the stability condition, $|T(\omega)|$ for $\omega \approx \omega_t$ can be approximated by

$$
|T(\omega)| \approx \frac{I_{CP} K_{VCO}}{2 \pi N} \frac{R_Z}{\omega}
$$
Stability / Loop Bandwidth Considerations

At the loop bandwidth frequency $\omega_t$, the loop transmission is unity.

Equating $|T(\omega_t)| = 1$ and solving for the loop bandwidth $\omega_t$ gives:

$$\omega_t \approx \frac{1}{2\pi N} \cdot K_{VCO} \cdot I_{CP}R_Z$$

Note that $I_{CP}R_Z$ product is a voltage that can be

- derived from a bandgap for temperature stability of $\omega_t$, or
- changed via $I_{CP}$ for adjustment of $\omega_t$
Summary: “Big Picture“ Key Concepts

• Time-frequency relationships among jitter characterization technique enable specification, design, measurement, simulation in most convenient domain.

• $\kappa$ expressions relate fundamental noise mechanisms to system-level jitter / phase noise performance.

• In general, increasing power / current / voltage swing improves jitter.

• To achieve fundamental limit of jitter performance, watch out for interference (e.g. substrate / supply noise coupling). May drive choice of delay stage (e.g. differential rather than single-ended).