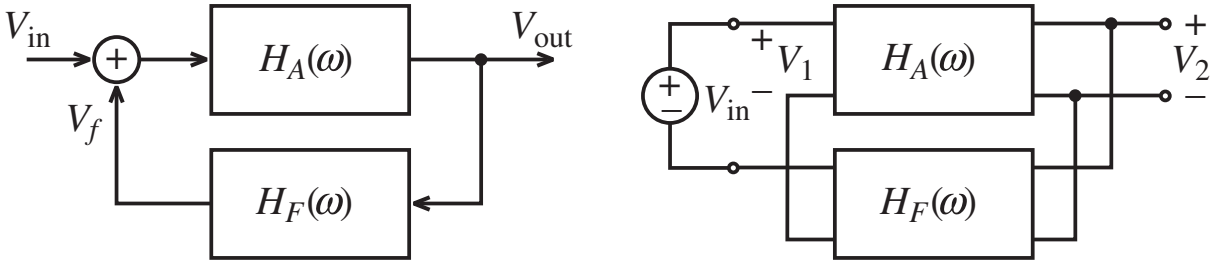
R. Ludwig and G. Bogdanov
"RF Circuit Design: Theory and Applications"
2nd edition

Figures for Chapter 10



(a) Closed-loop circuit model (b) Network representation

Figure 10-1 Basic oscillator configuration.

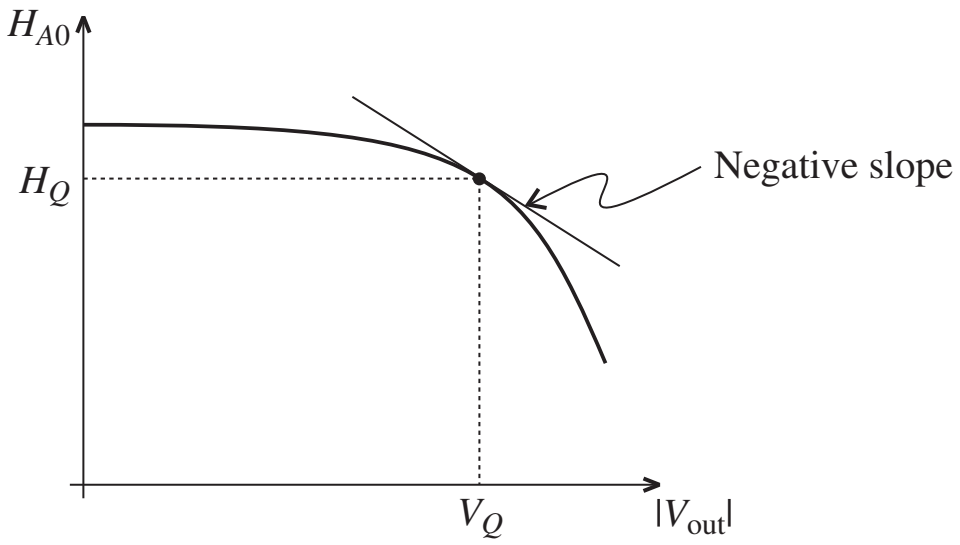


Figure 10-2 Output voltage versus gain characteristic.

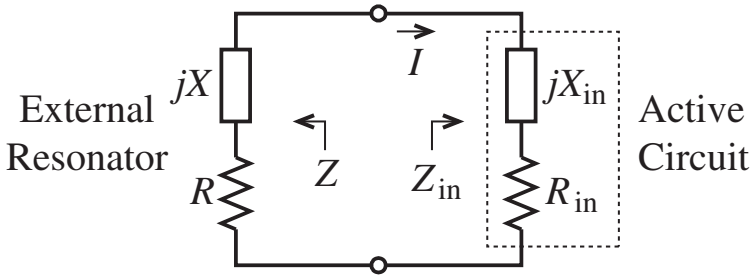


Figure 10-3 Generic negative resistance oscillator circuit.

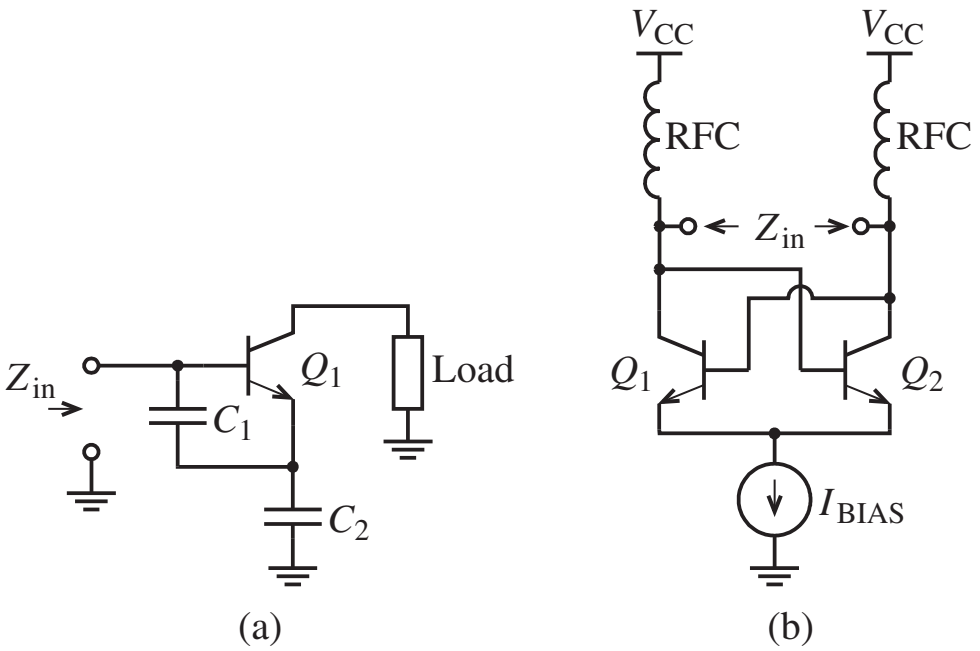


Figure 10-4 Common negative resistance circuits for oscillators: (a) emitter/source feedback (no biasing shown) and (b) cross-coupled.

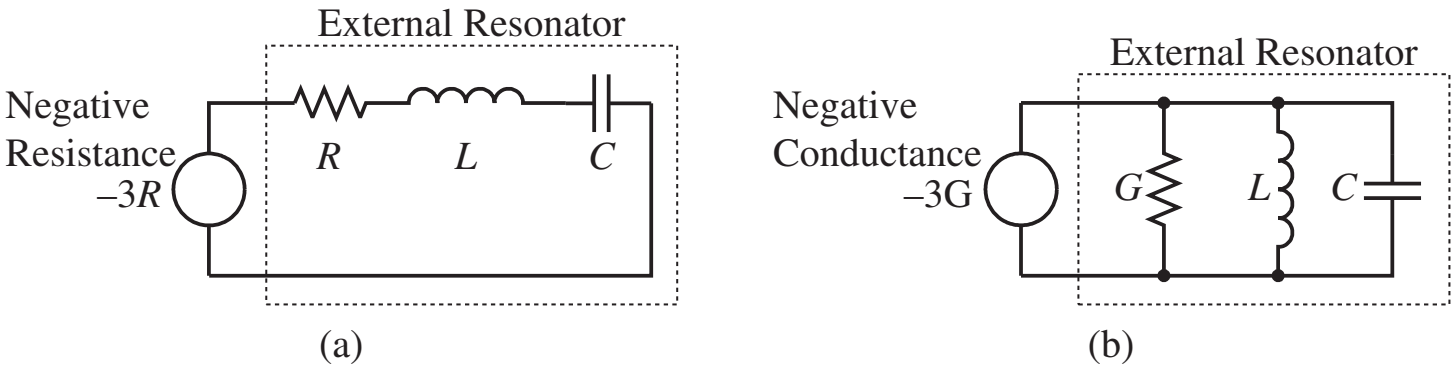


Figure 10-5 Negative resistance oscillator (a) and negative conductance oscillator (b).

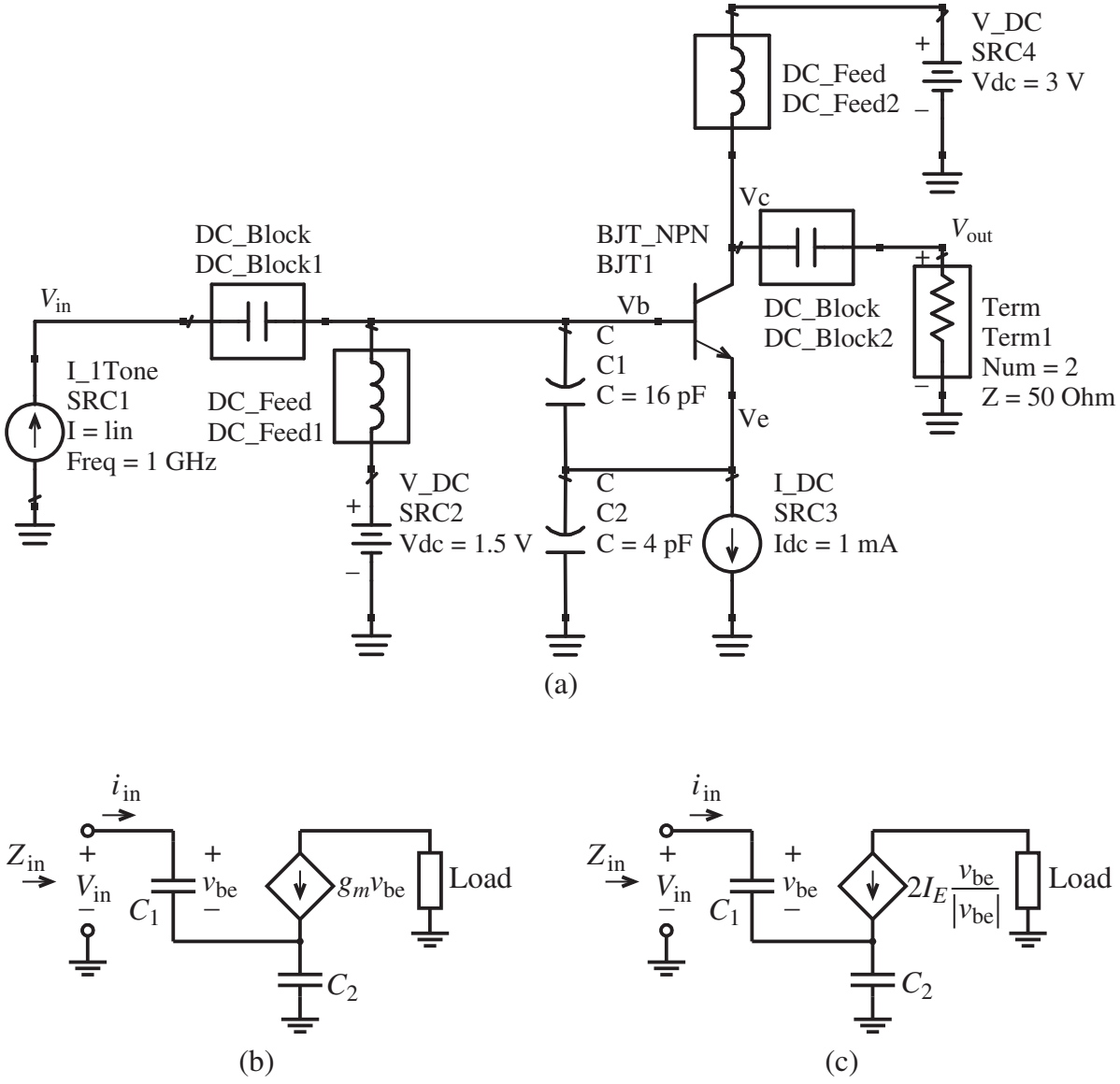


Figure 10-6 Negative resistance circuit using emitter feedback: (a) ADS schematic including biasing, (b) small-signal model, and (c) large-signal model at the first harmonic frequency. For the ADS model legend, see next page.

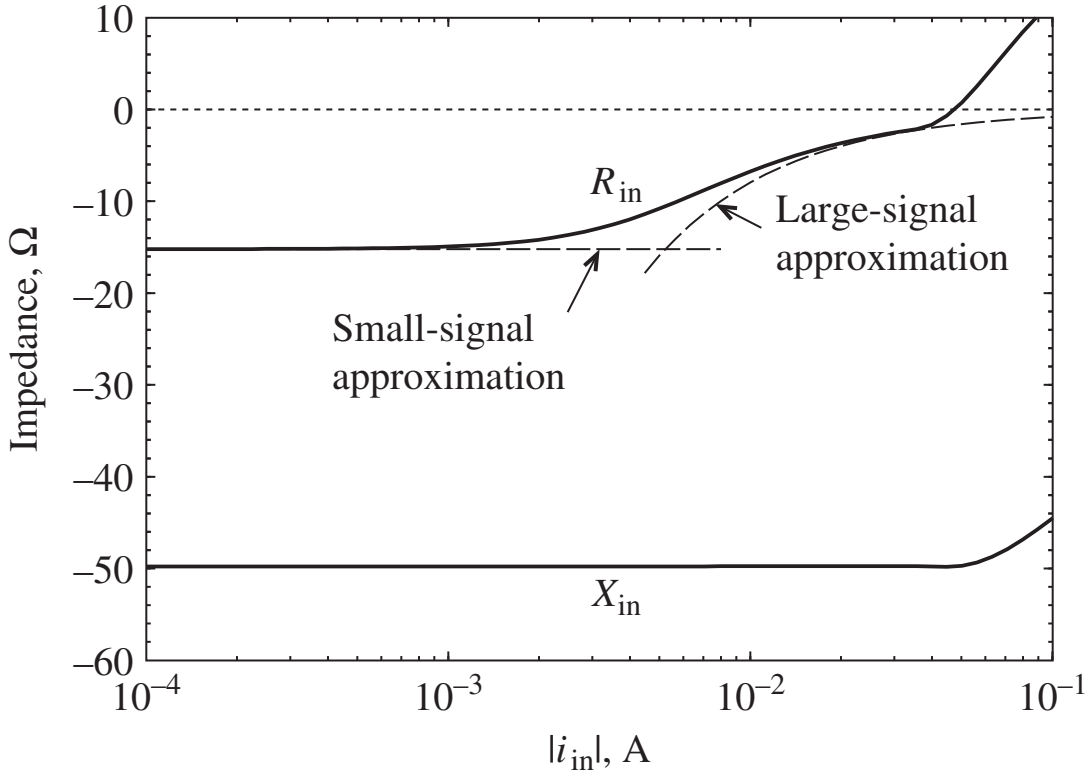


Figure 10-7 Harmonic Balance simulation results for the example emitter feedback circuit at 1 GHz.

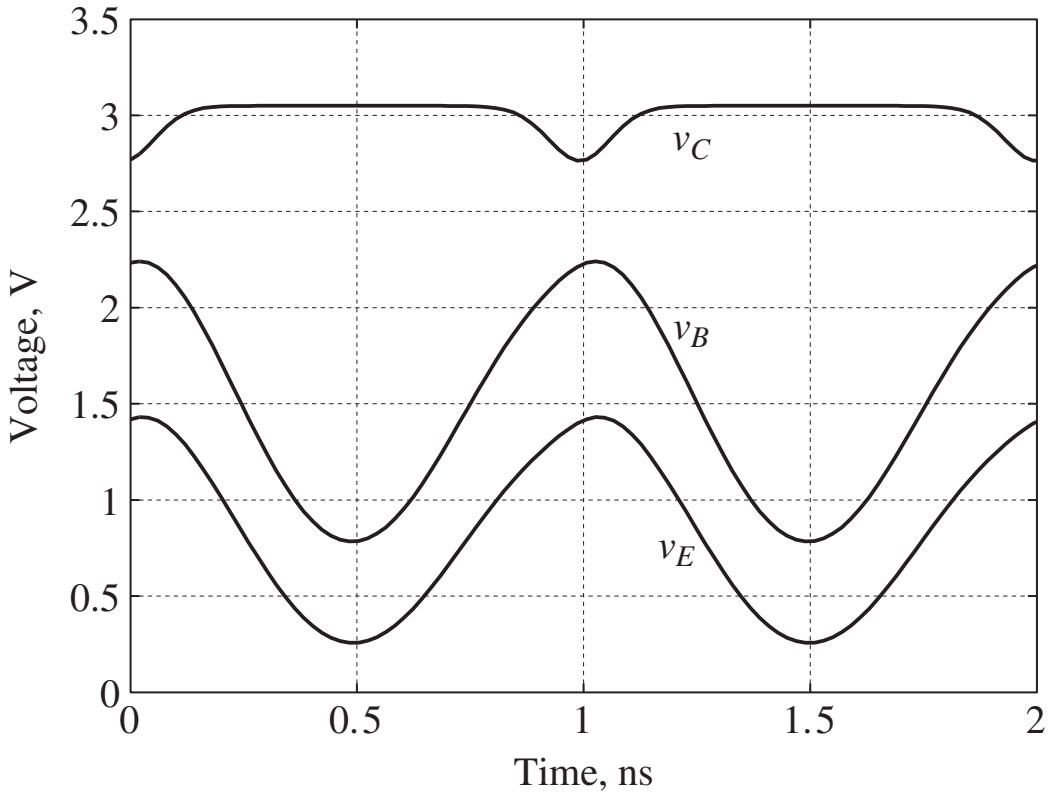


Figure 10-8 Harmonic Balance simulation of a 1 GHz oscillator with the emitter feedback negative resistance circuit.

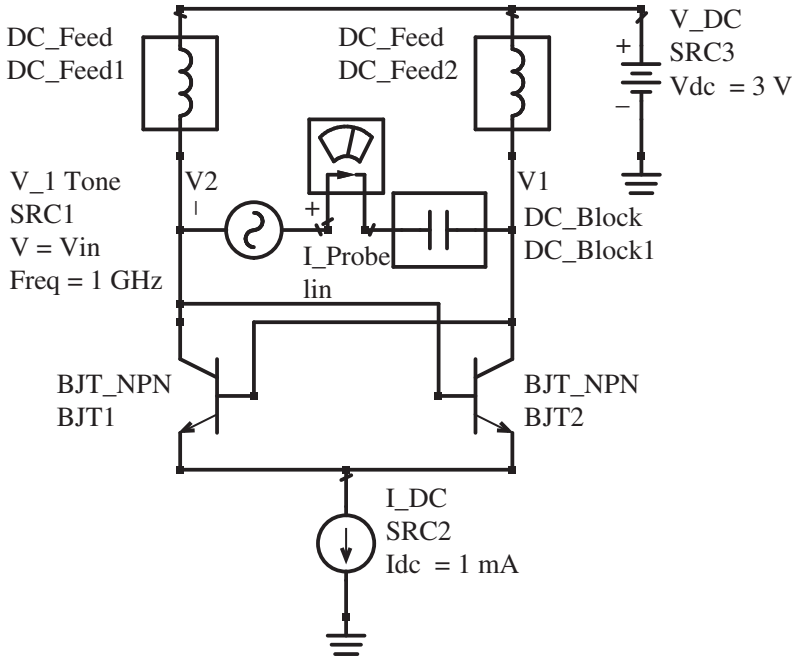


Figure 10-9 Cross-coupled pair with biasing, creating negative resistance.

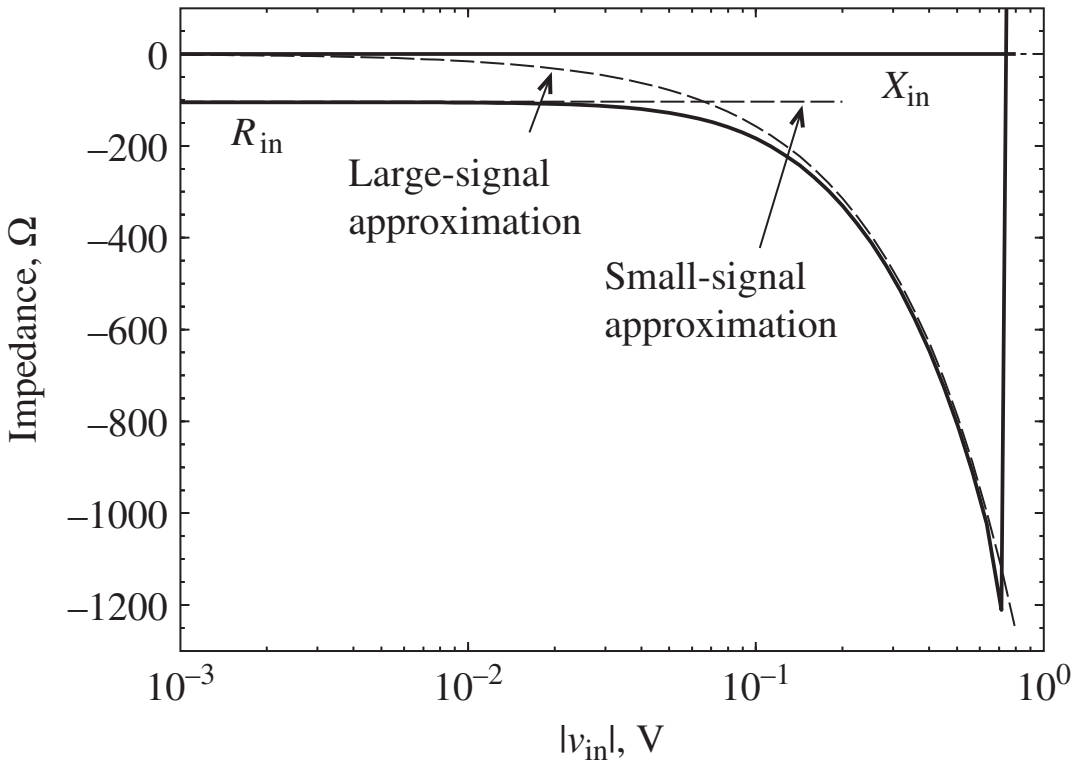


Figure 10-10 Harmonic balance simulation results for the example cross-coupled negative resistance circuit at 1 GHz.

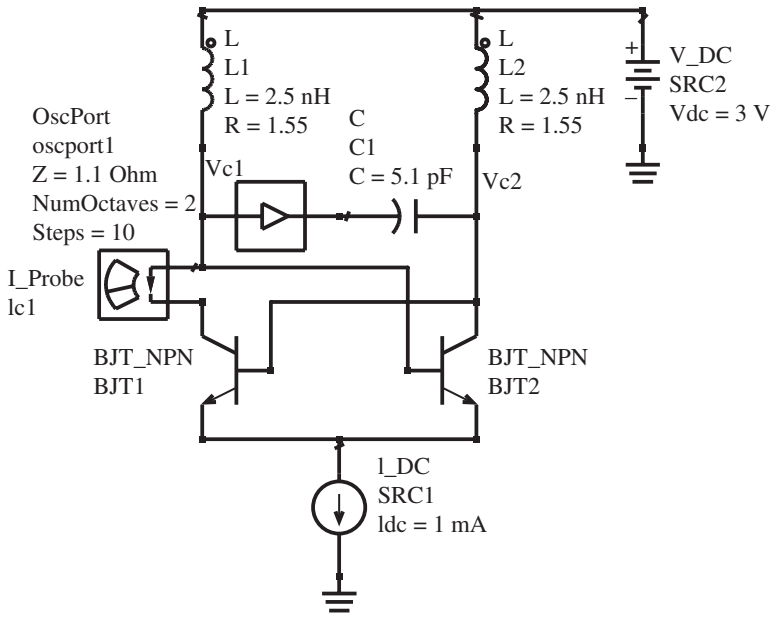


Figure 10-11 Cross-coupled oscillator. OscPort and I_Probe are simulator features that behave as short circuits.

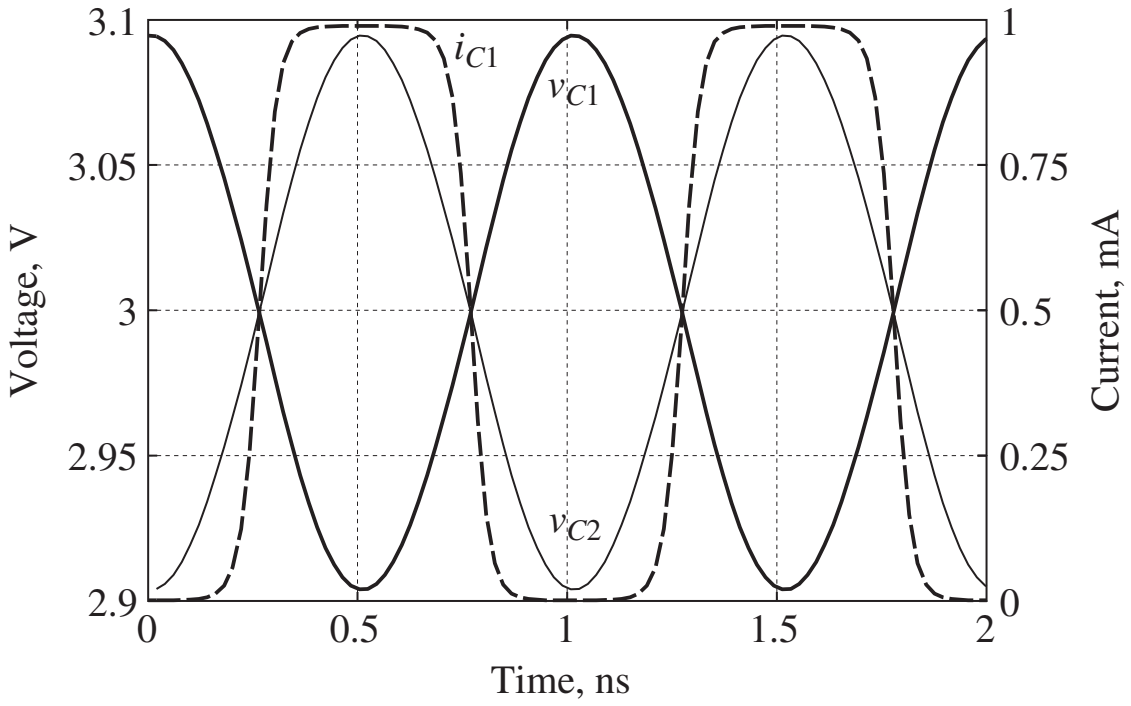


Figure 10-12 Harmonic balance simulation of a 1 GHz cross-coupled oscillator.

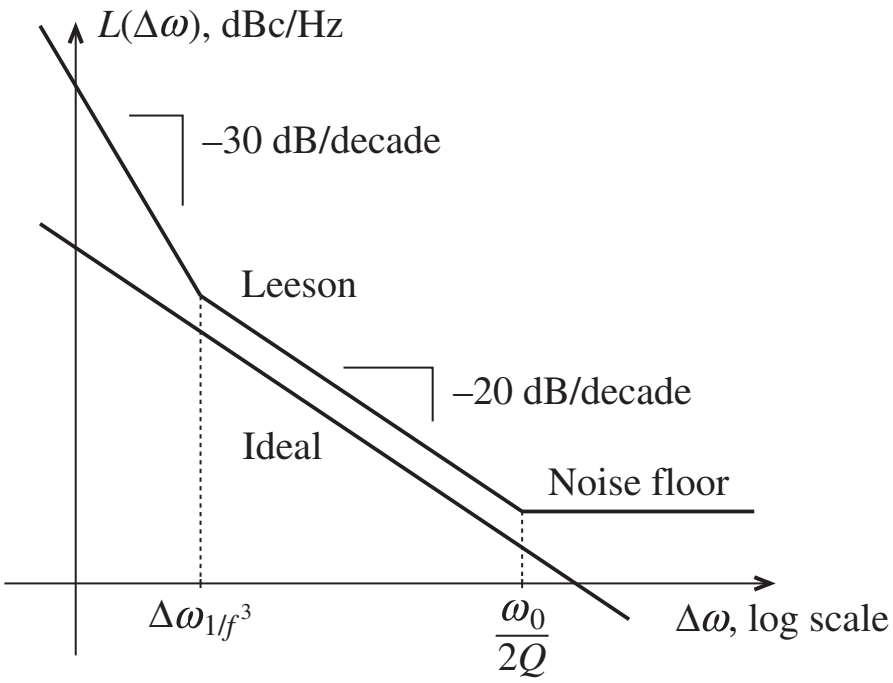


Figure 10-13 Oscillator phase noise according to Leeson's model and the ideal oscillator model.

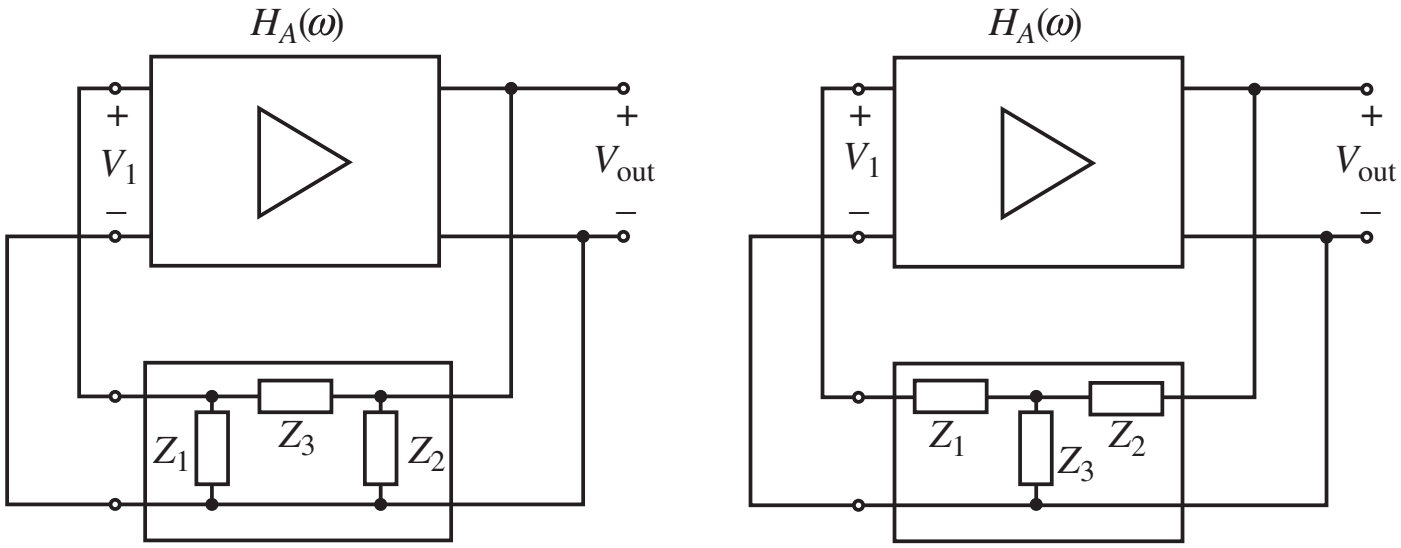


Figure 10-14 Feedback circuits with Pi- and T-type feedback loops.

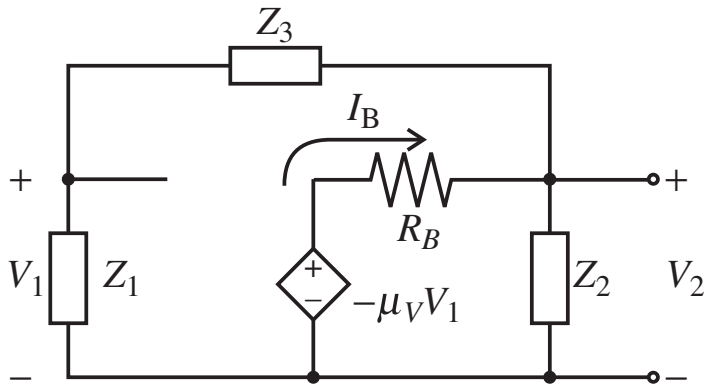
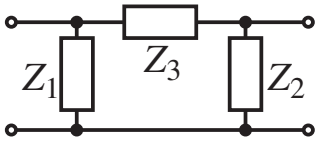
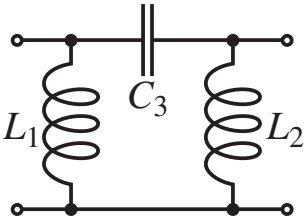
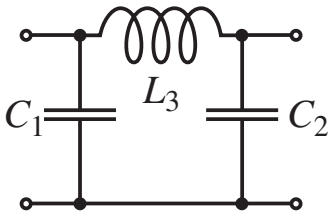
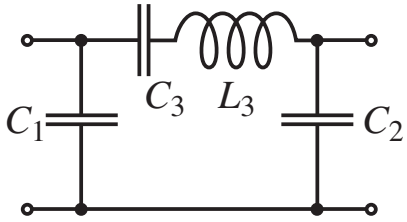


Figure 10-15 Feedback oscillator with FET electric circuit model.

Table 10-1 Various feedback configurations for oscillator designs based on Figure 14(a)

X_1, X_2		
X_3		
	 Hartley	 Colpitts  Clapp

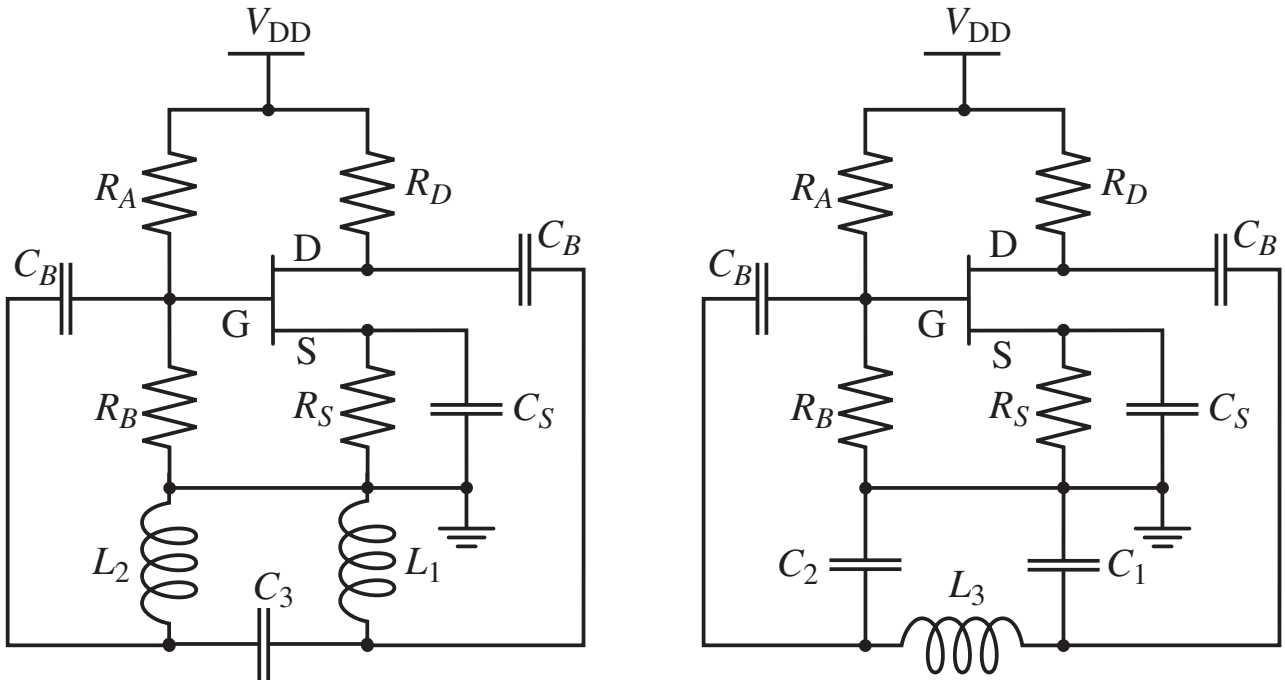


Figure 10-16 Hartley and Colpitts oscillators.

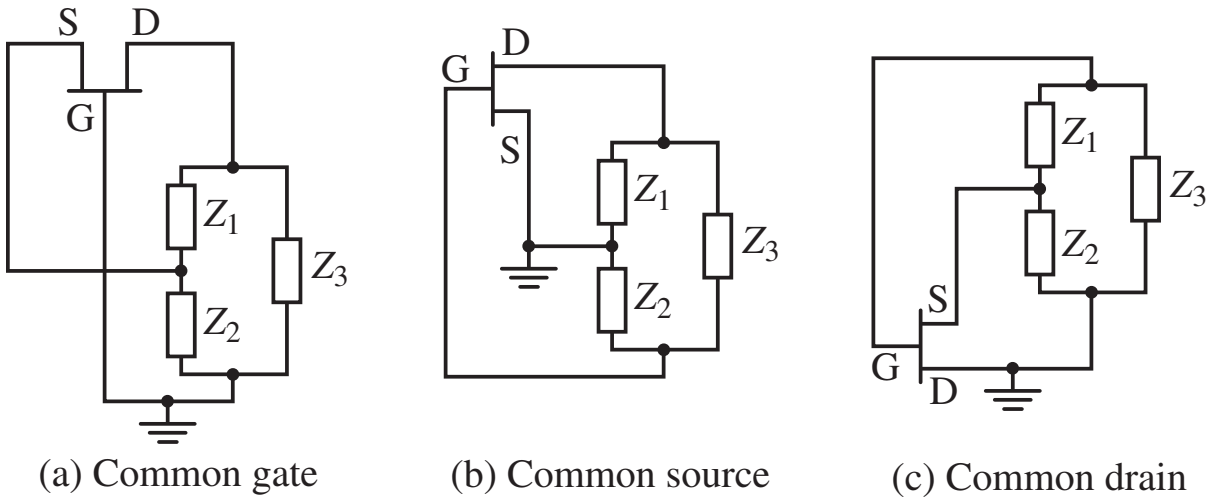


Figure 10-17 Common gate, source, and drain configurations.

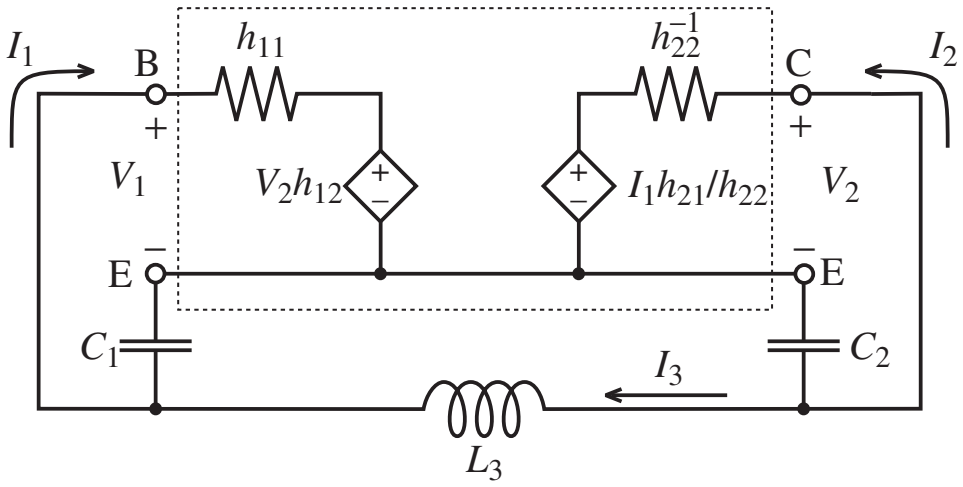


Figure 10-18 Colpitts oscillator design.

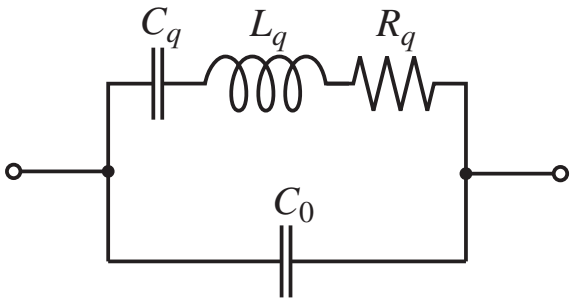


Figure 10-19 Quartz resonator equivalent electric circuit representation.

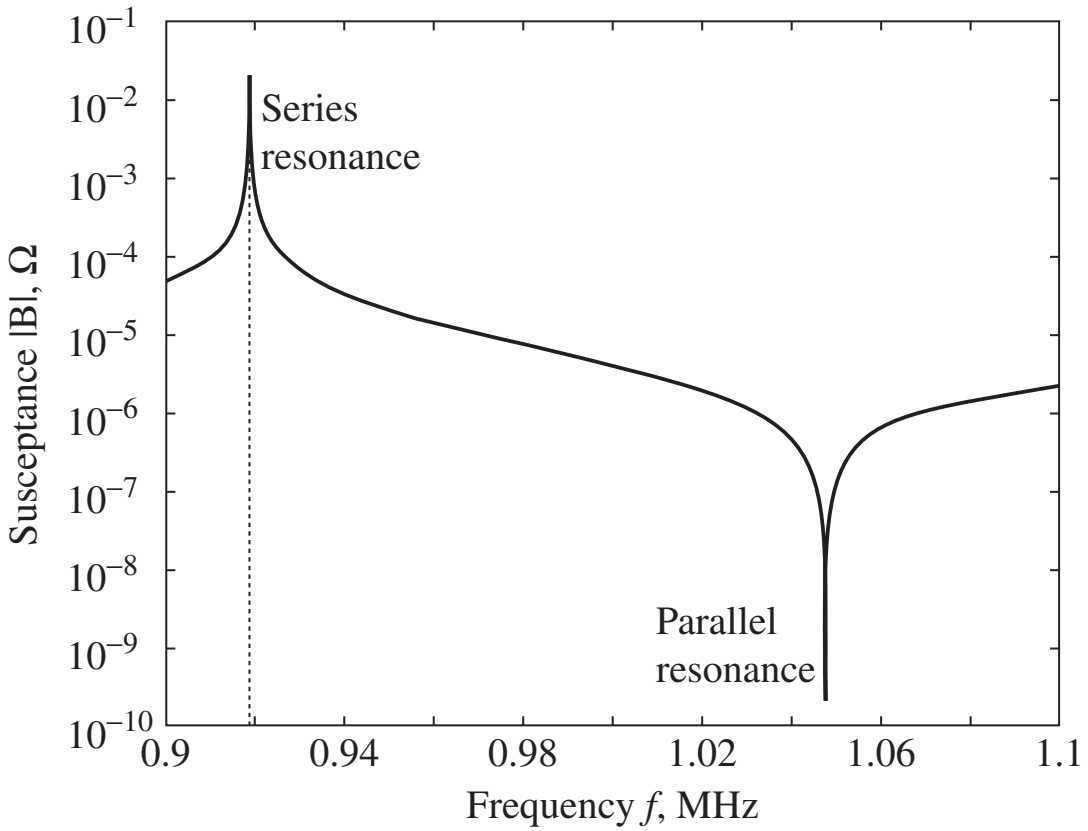
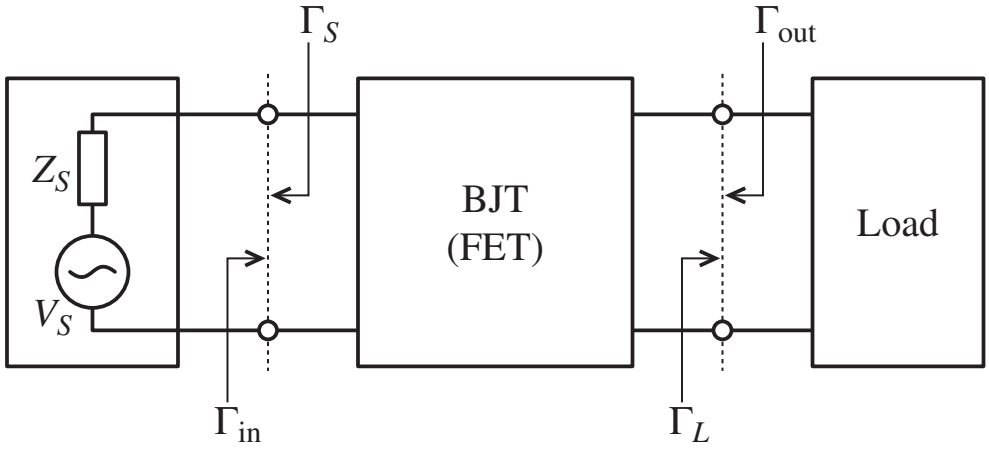
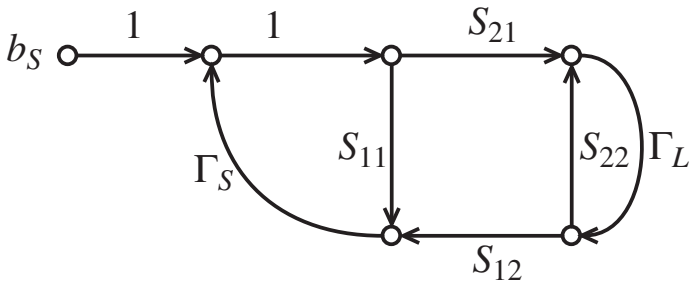


Figure 10-20 Susceptance response of a quartz element.



(a) Sourced and loaded transistor



(b) Equivalent signal flow graph

Figure 10-21 Sourced and loaded transistor and its flow graph model.

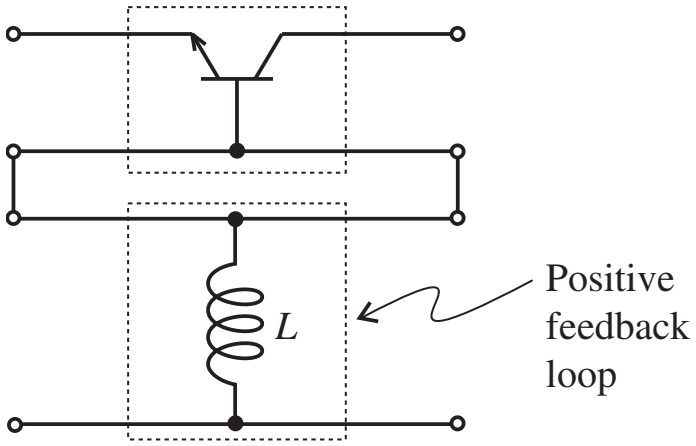


Figure 10-22 Network representation of the BJT with base inductance.

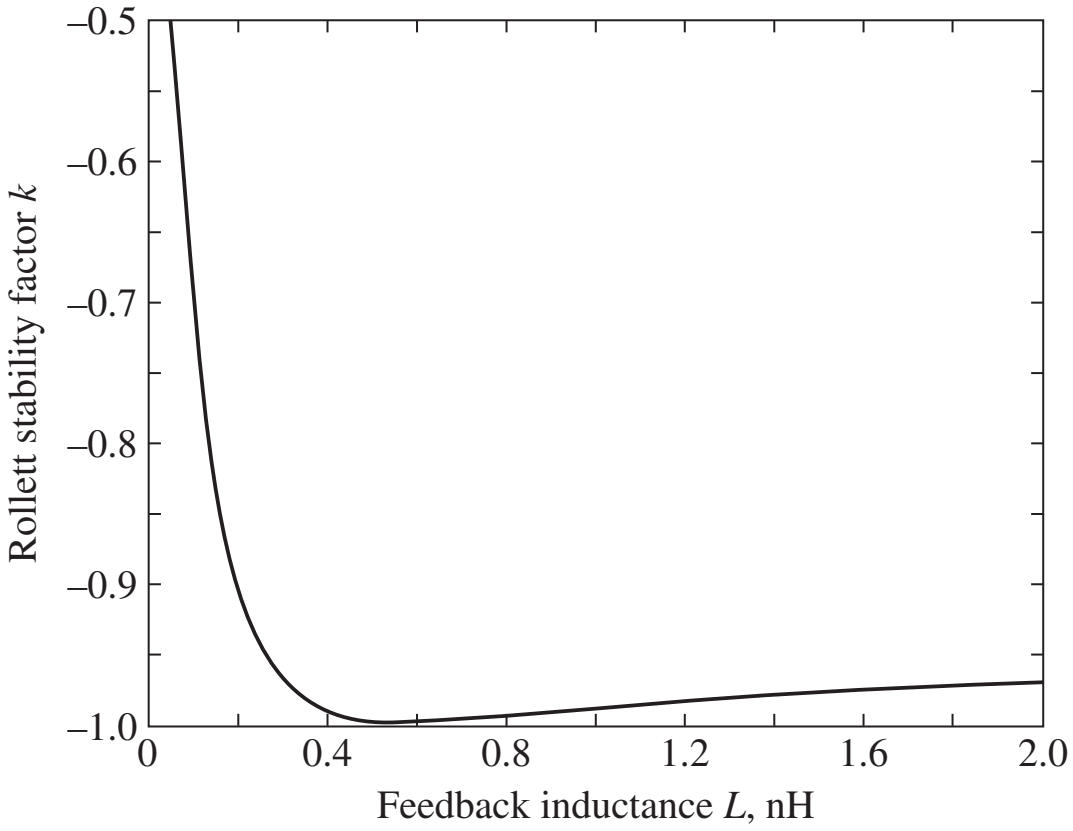


Figure 10-23 Rollett stability factor (*k*) as a function of feedback inductance in common-base configuration.

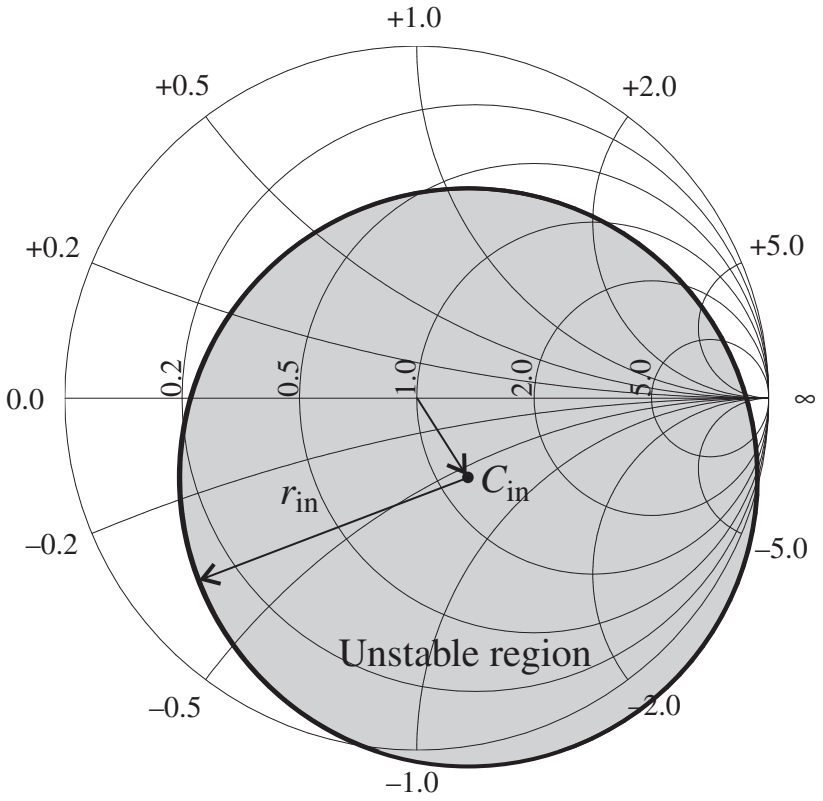


Figure 10-24 Input stability circle for the oscillator design.

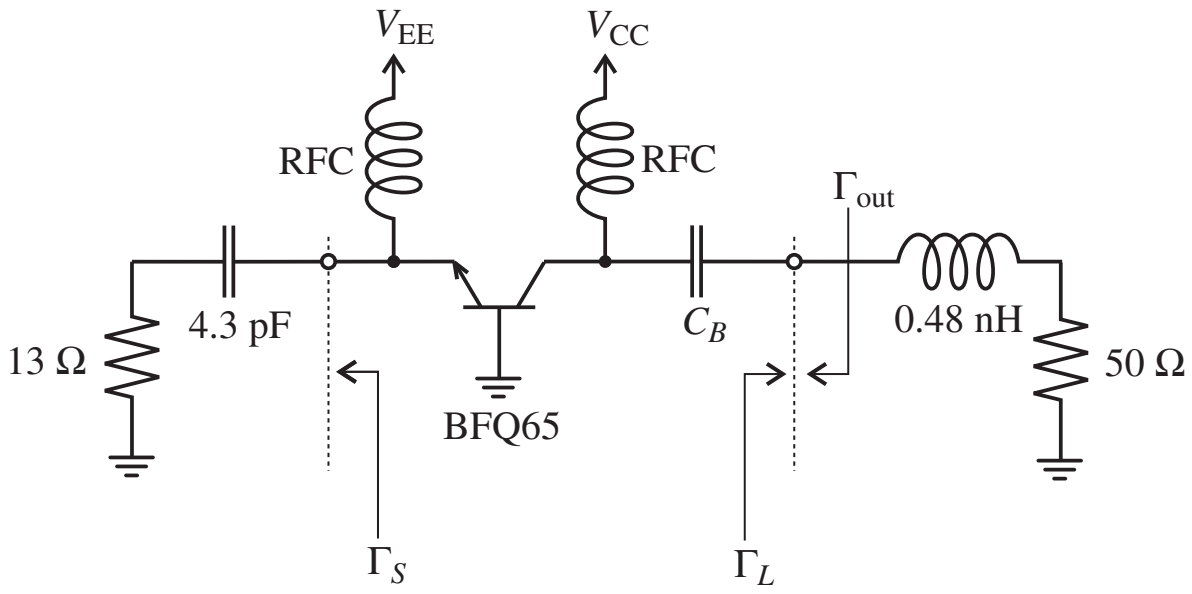


Figure 10-25 Series-feedback BJT oscillator circuit.

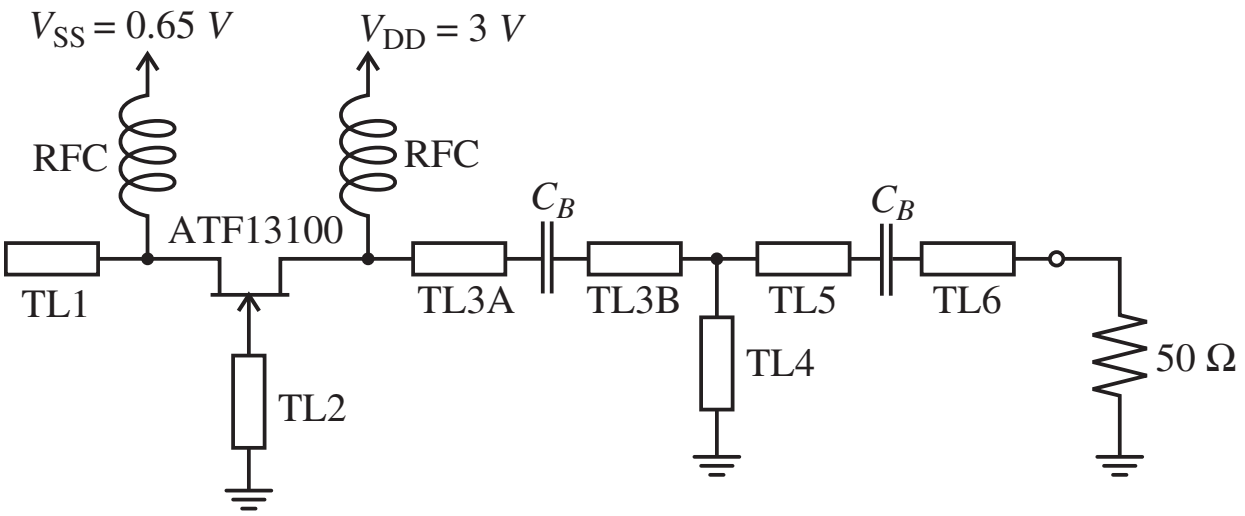


Figure 10-26 GaAs FET oscillator implementation with microstrip lines.

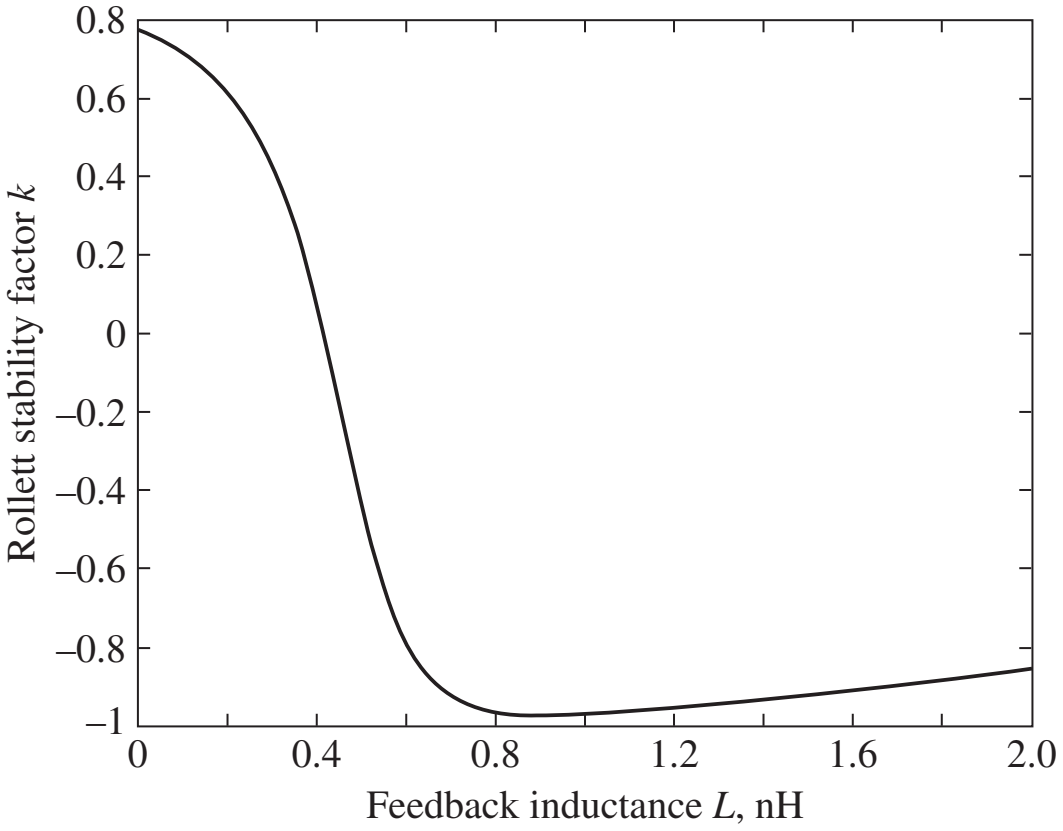


Figure 10-27 Stability factor for FET in common-gate configuration as a function of gate inductance.

Table 10-2 Dimensions of the transmission lines in the FET oscillator

Transmission line	Electrical length, deg.	Width, mil	Length, mil
TL1	80	74	141
TL2	48.5	74	86
TL3	67	74	118
TL4	66	74	116

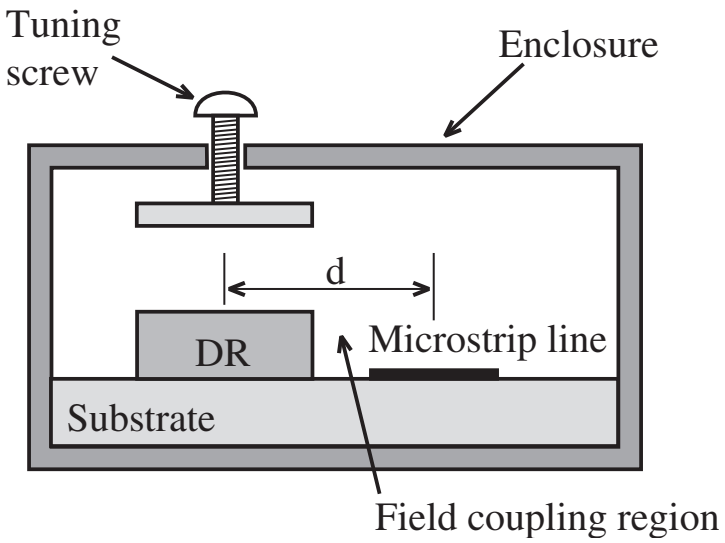
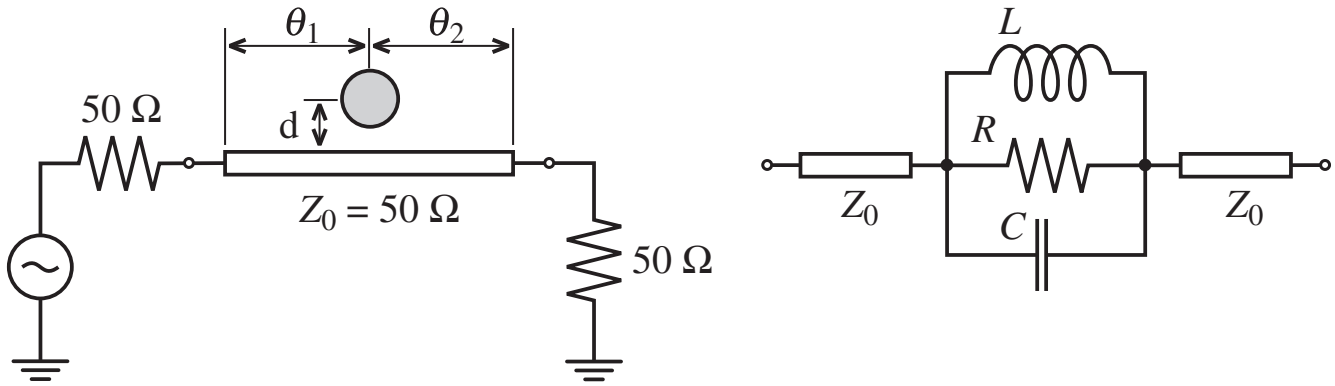


Figure 10-28 Dielectric resonator (DR) placed in proximity to a microstrip line.



(a) Terminated microstrip line with DR (b) Transmission line model

Figure 10-29 Placement of DR along a transmission line and equivalent circuit representation for *S*-parameter computation.

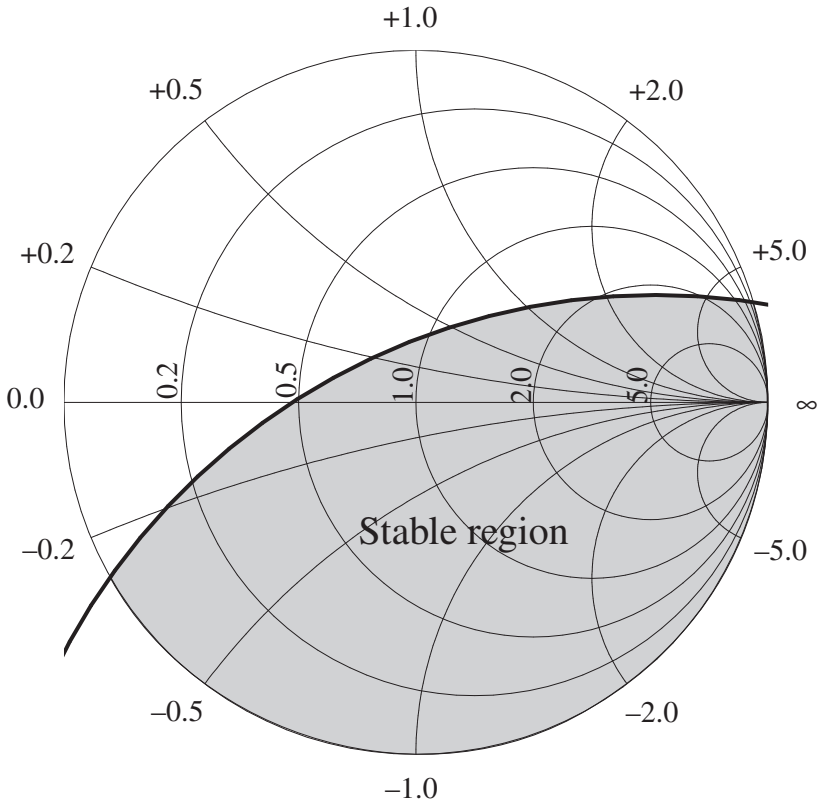


Figure 10-30 Input stability circle of the FET in the DRO design example.

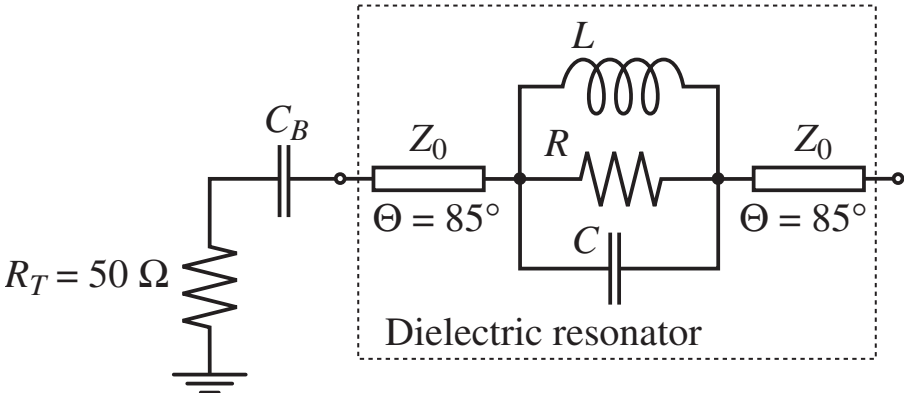
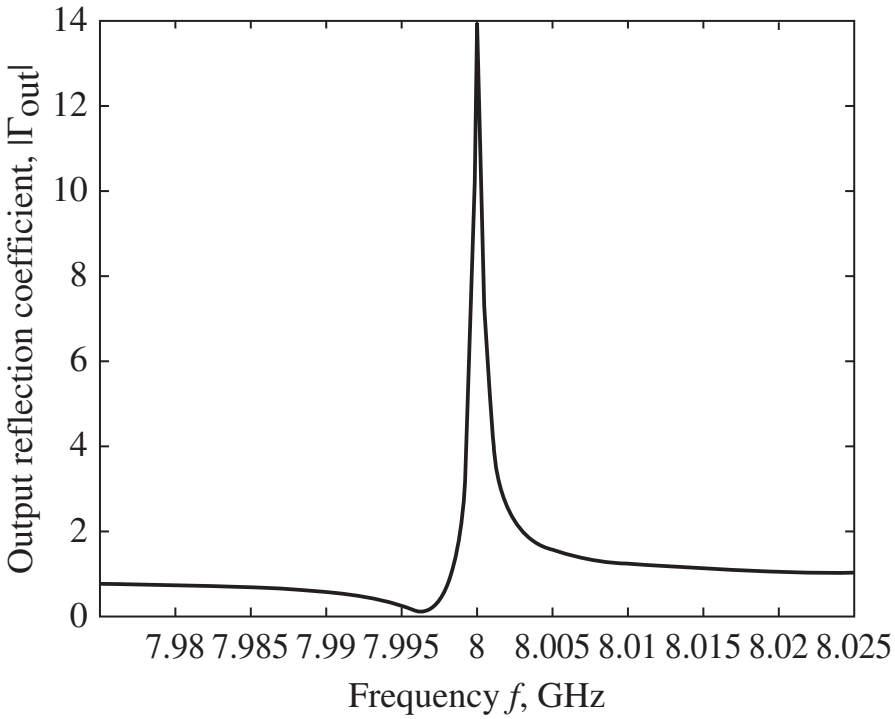
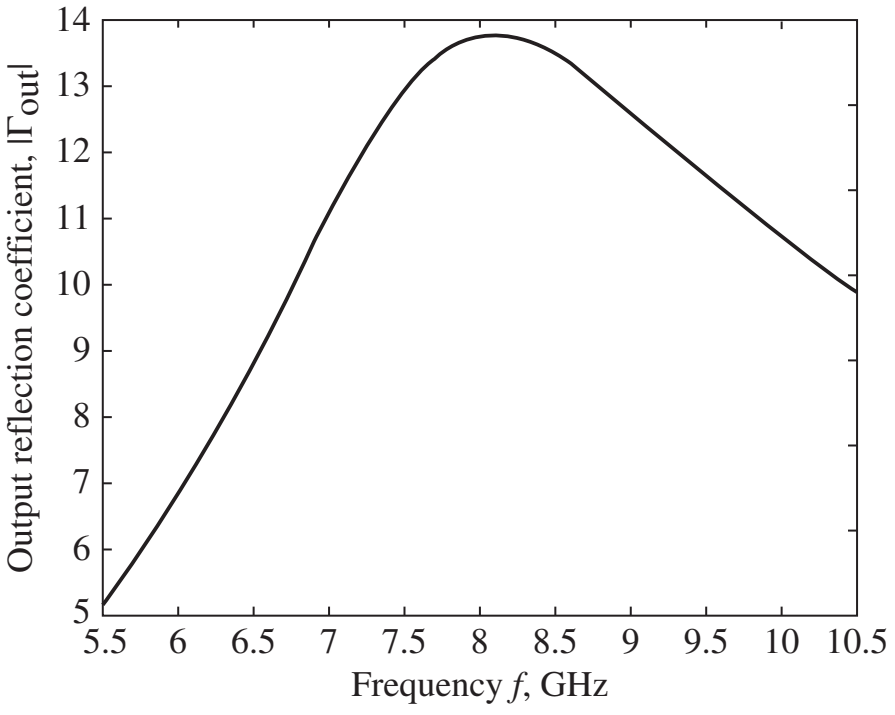


Figure 10-31 DR-based input matching network of the FET oscillator.



(a) Oscillator design with DR



(b) Conventional oscillator without DR

Figure 10-32 Frequency response of the output reflection coefficient for an oscillator design with and without DR.

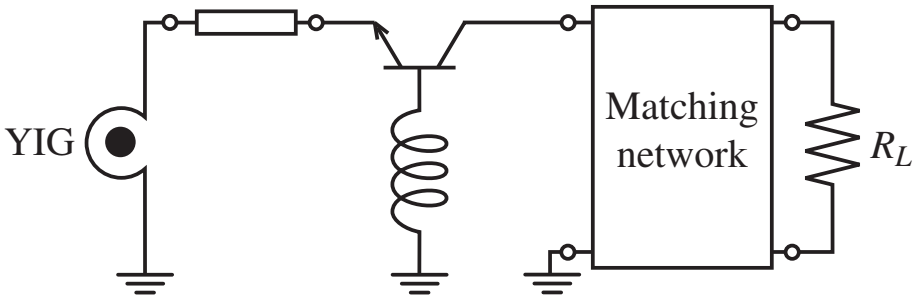
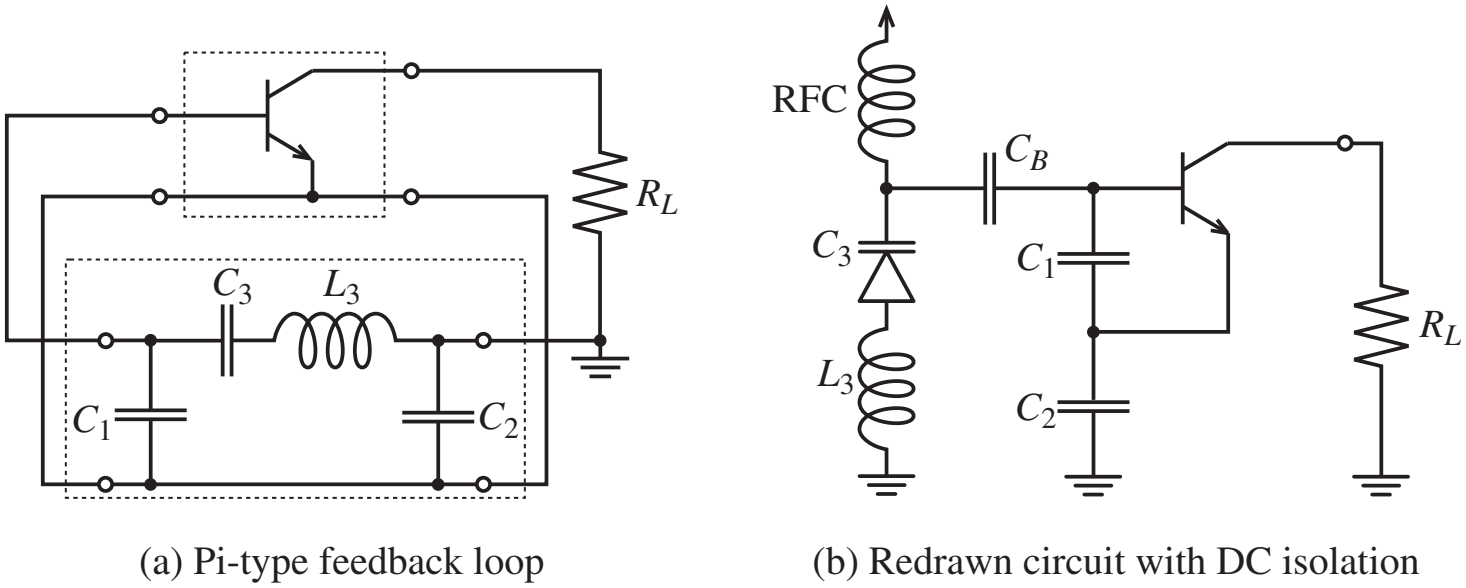


Figure 10-33 Oscillator design based on a YIG tuning element.



(a) Pi-type feedback loop

(b) Redrawn circuit with DC isolation

Figure 10-34 Varactor diode oscillator.

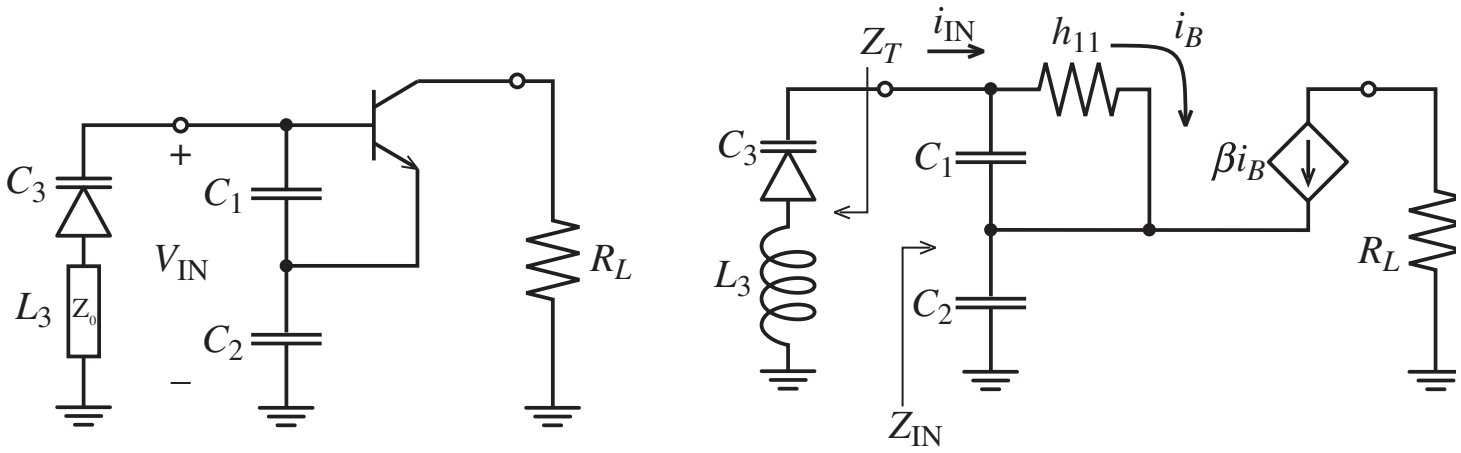
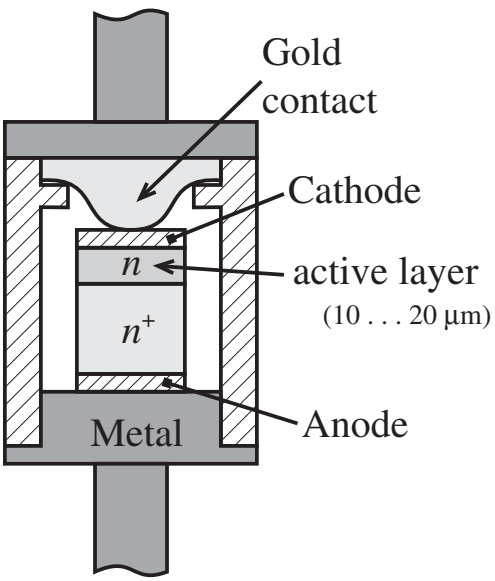
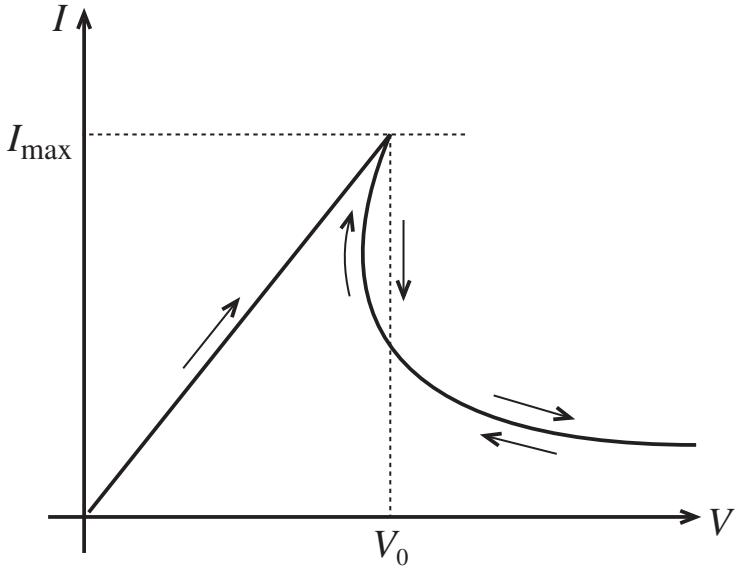


Figure 10-35 Circuit analysis of varactor diode oscillator.



(a) Gunn element structure



(b) Current vs. applied voltage response

Figure 10-36 Gunn element and current versus voltage response.

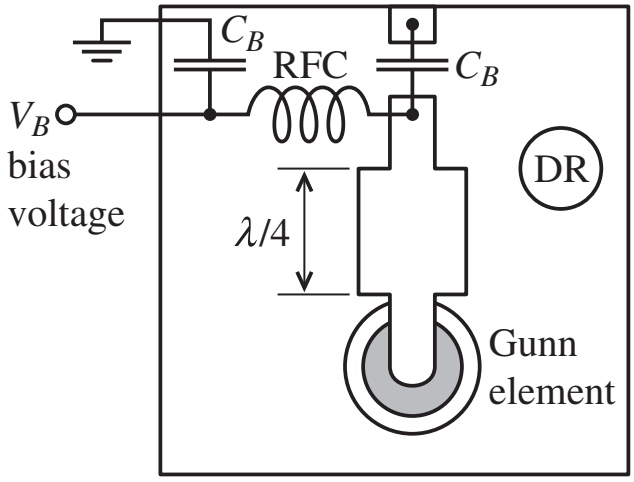


Figure 10-37 Gunn element oscillator circuit with dielectric resonator (DR).

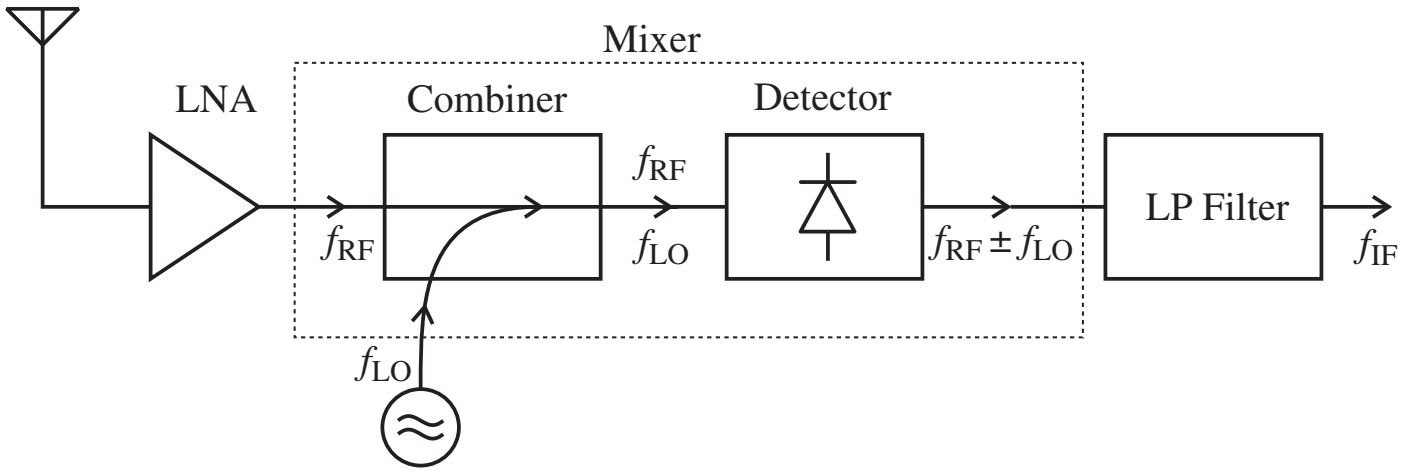


Figure 10-38 Heterodyne receiver system incorporating a mixer.

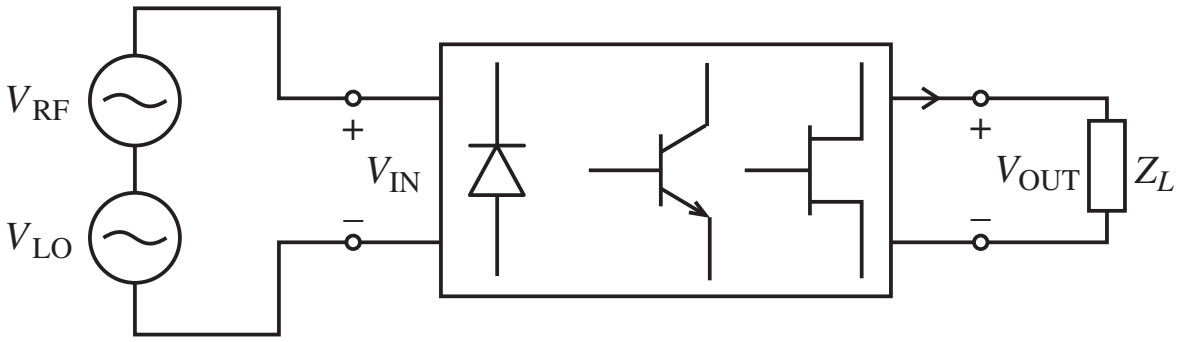


Figure 10-39 Basic mixer concept: two input frequencies are used to create new frequencies at the output of the system.

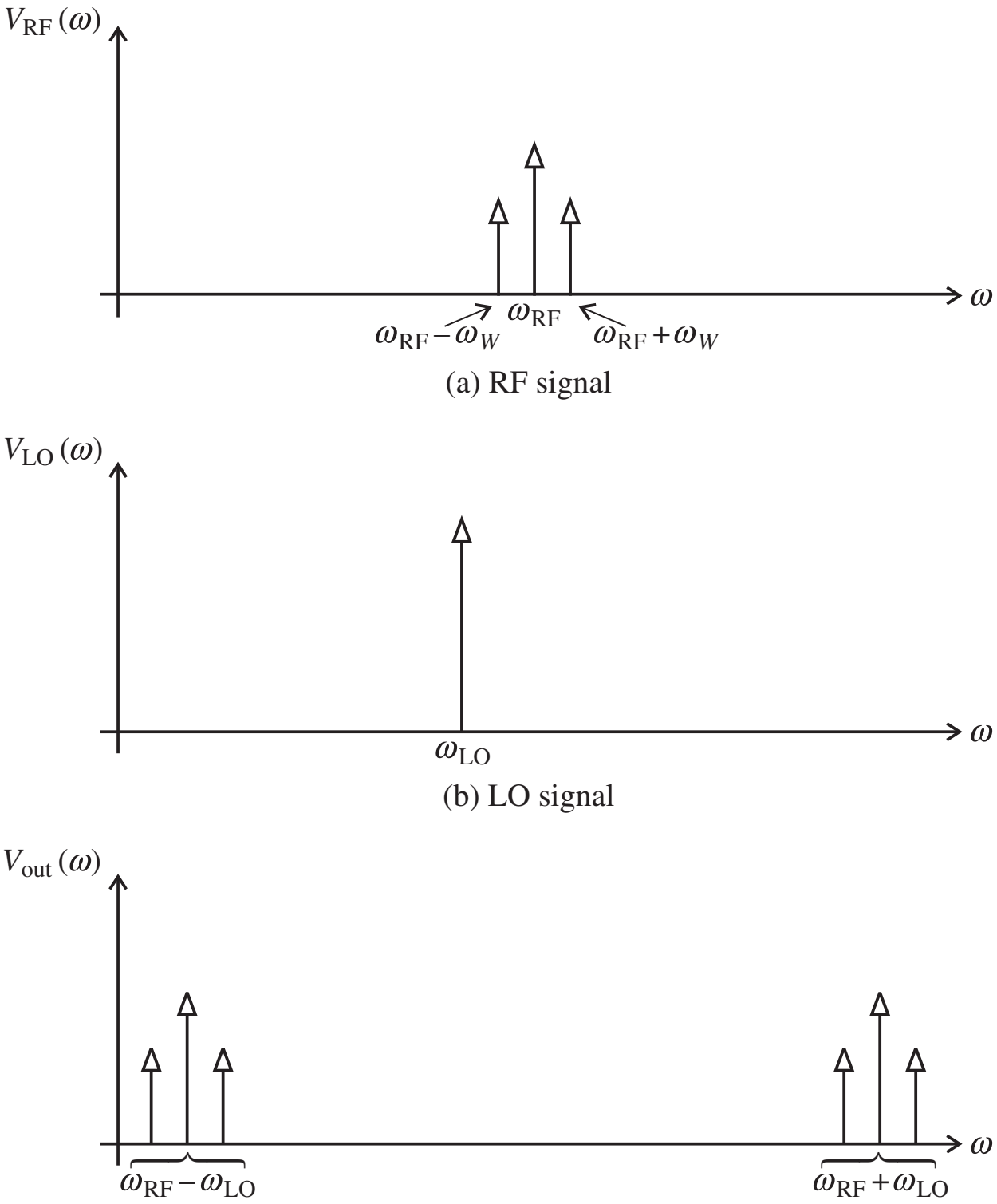


Figure 10-40 Spectral representation of mixing process.

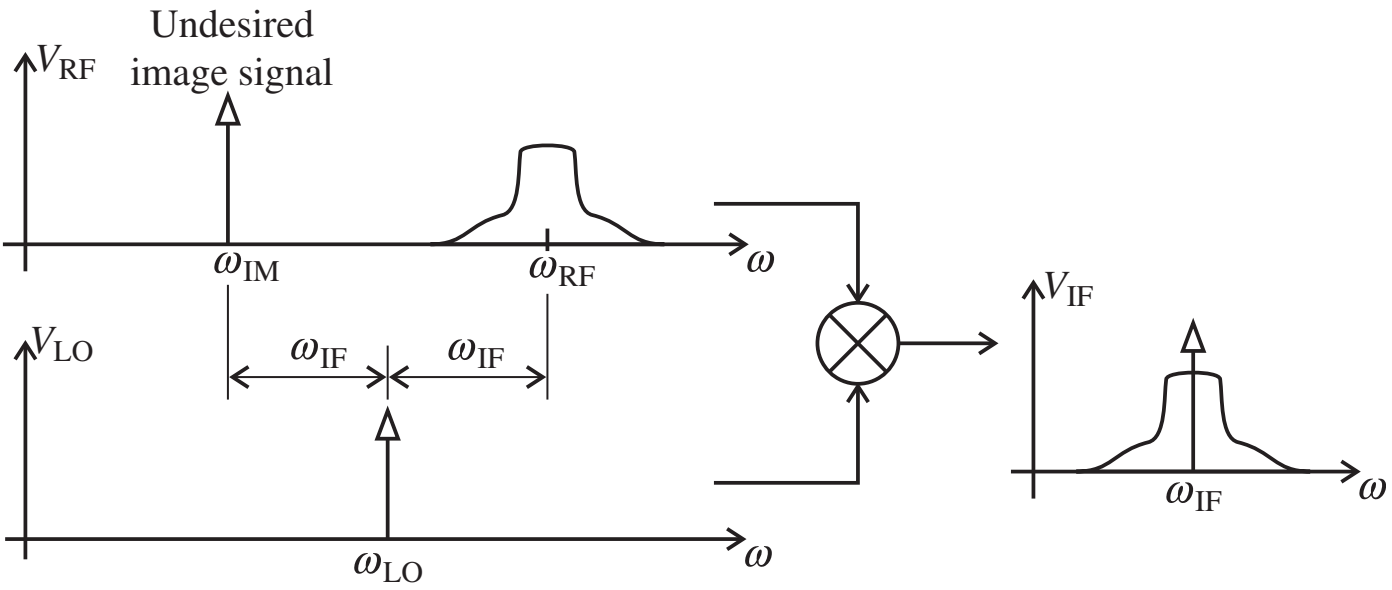
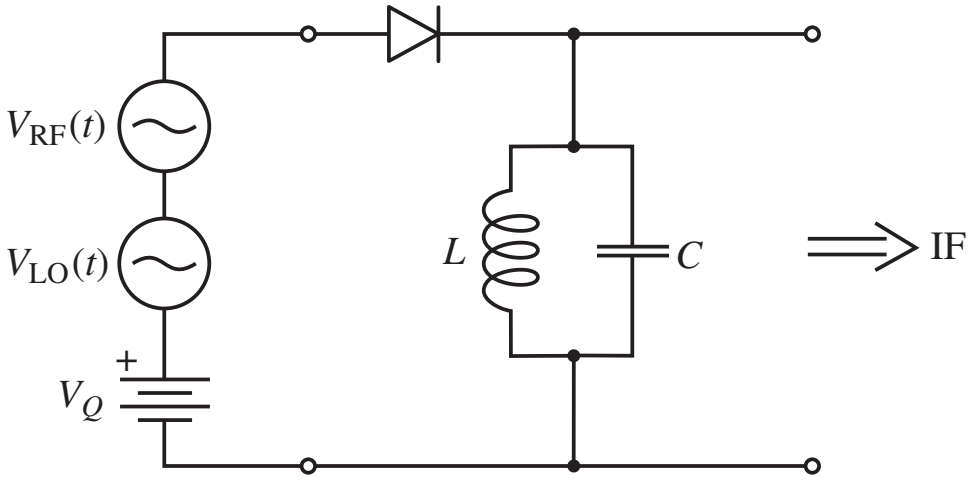
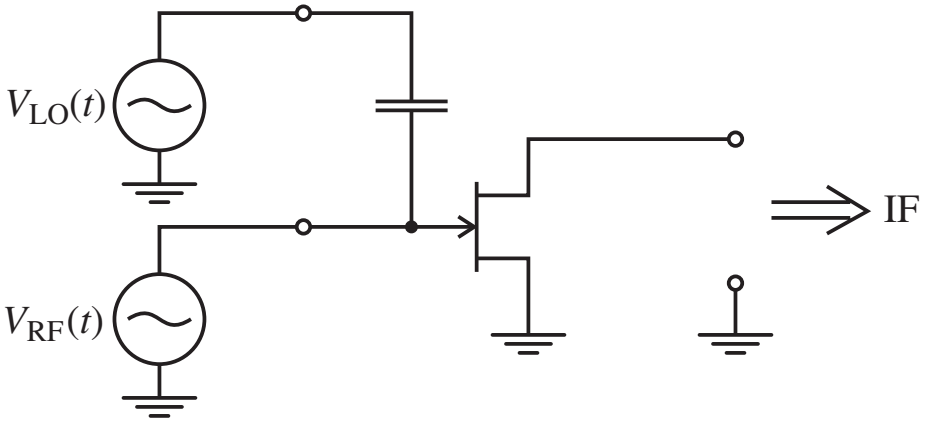


Figure 10-41 Problem of image frequency mapping.



(a) Diode mixer



(b) FET mixer

Figure 10-42 Two single-ended mixer types.

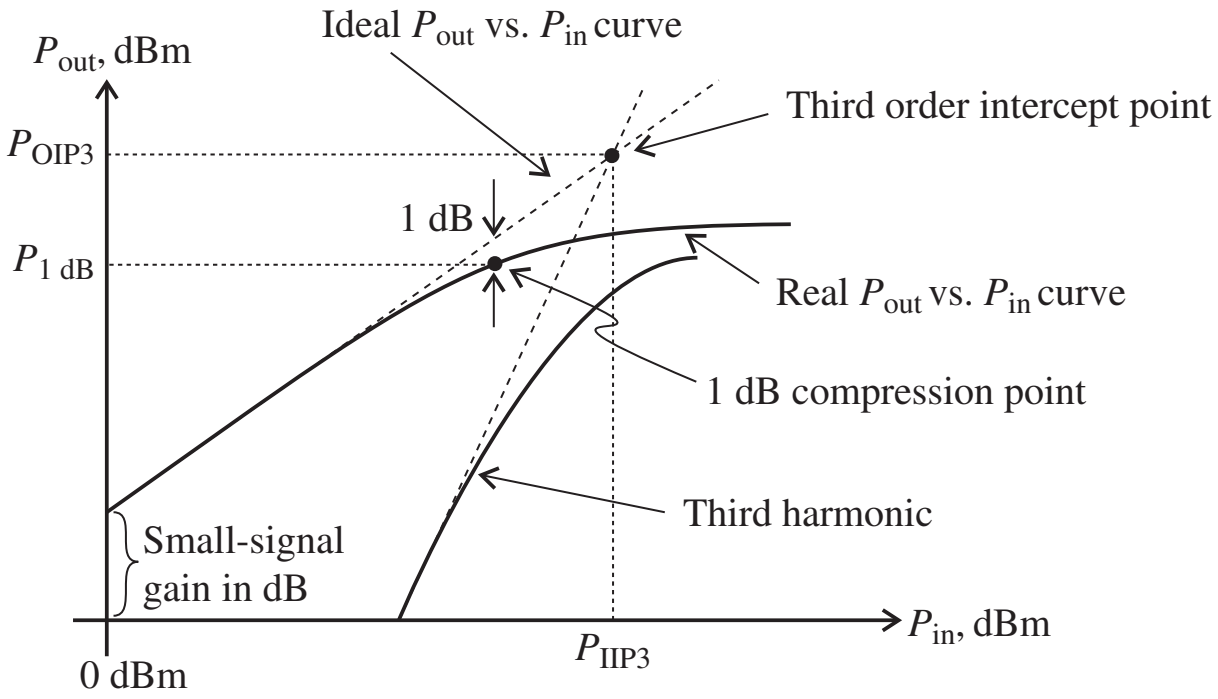


Figure 10-43 Conversion compression and intermodulation product of a mixer.

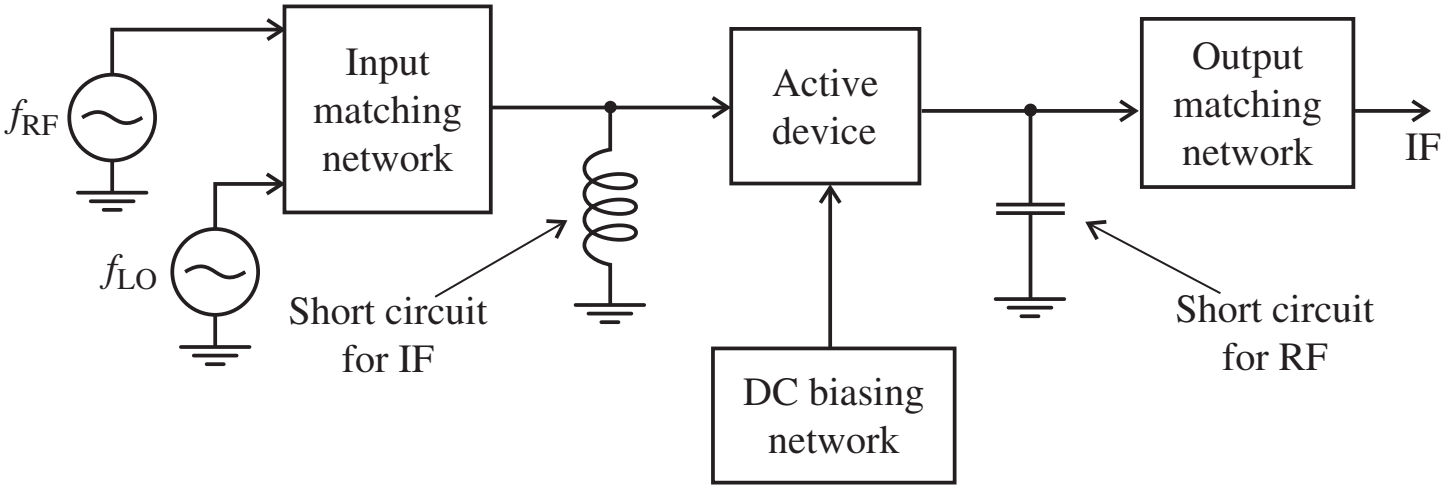


Figure 10-44 General single-ended mixer design approach.

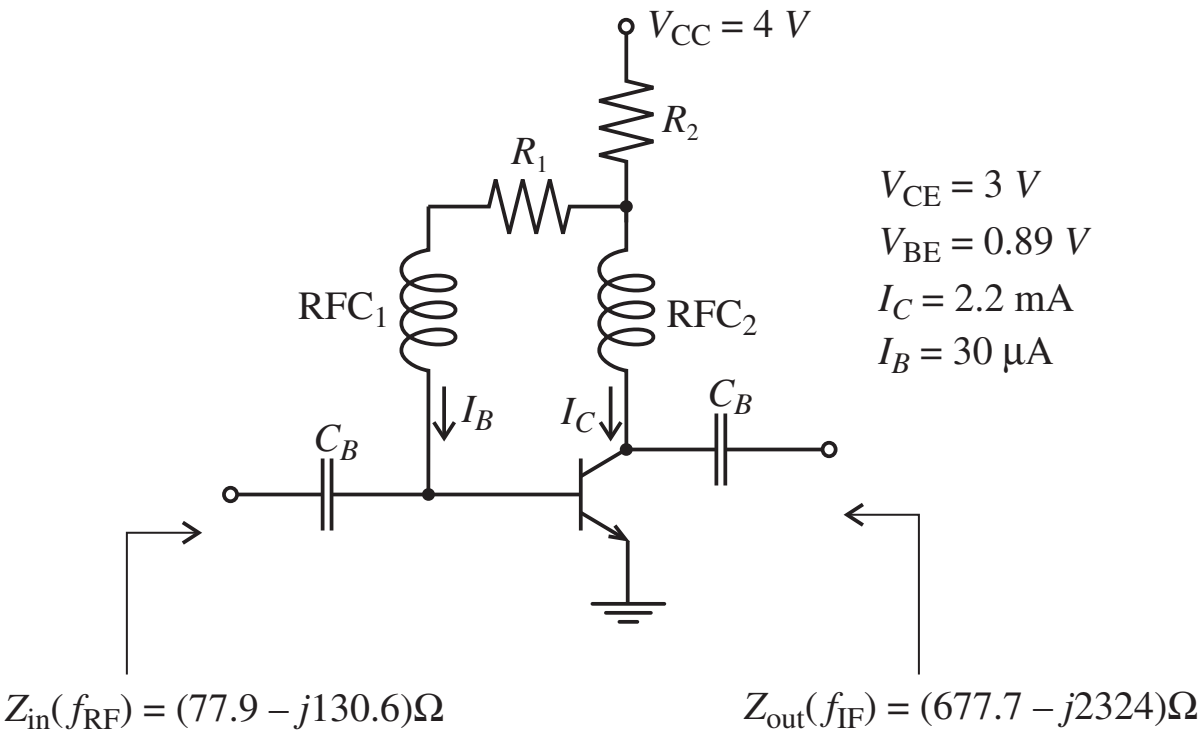


Figure 10-45 DC-biasing network for BJT mixer design.

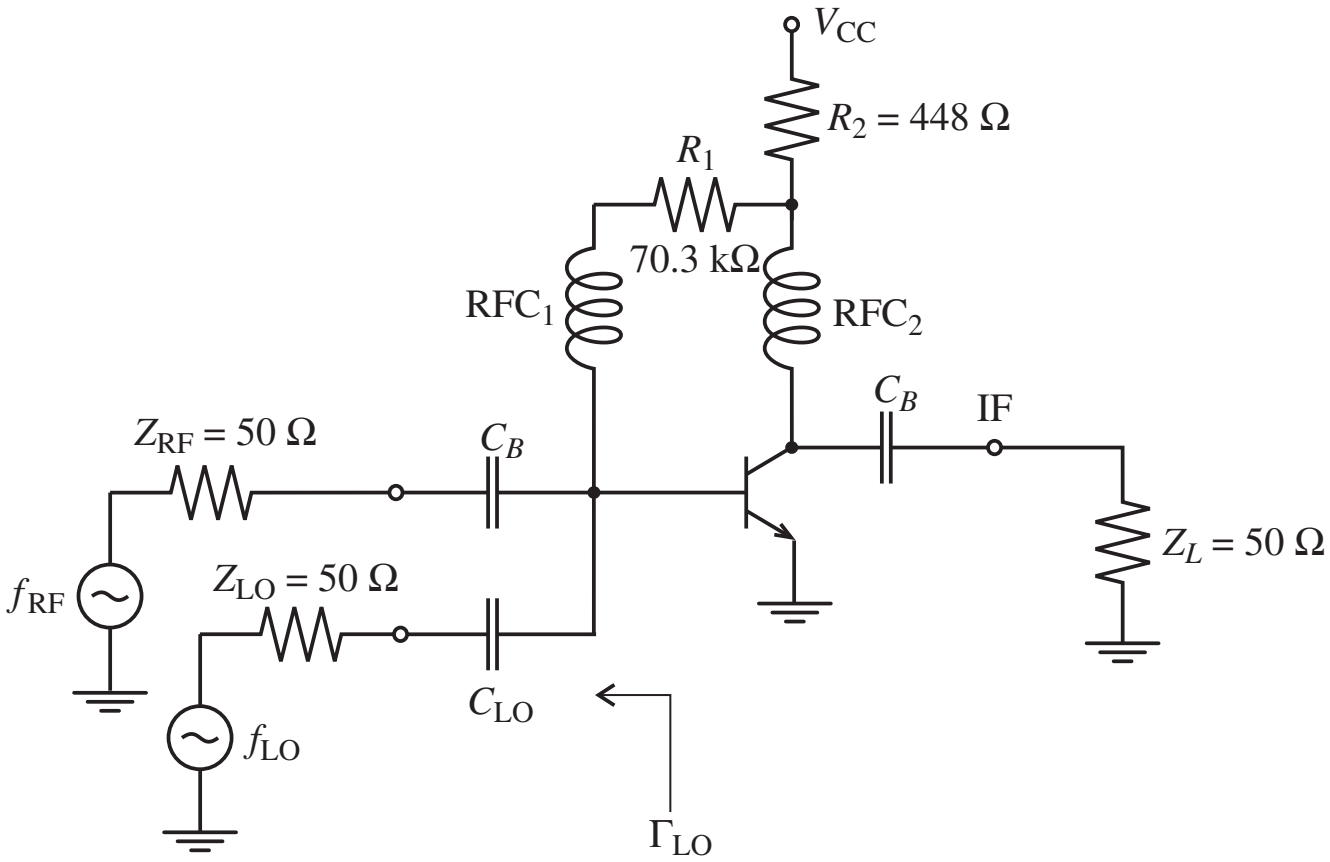


Figure 10-46 Connection of RF and LO sources to the BJT.

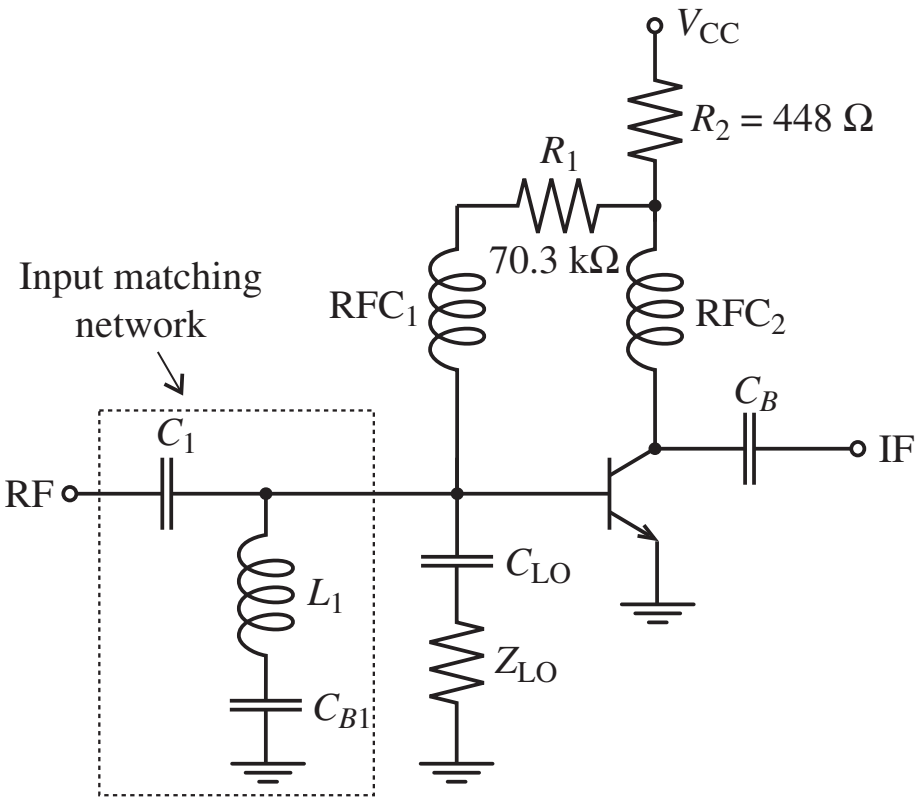


Figure 10-47 Input matching network for a single-ended BJT mixer.

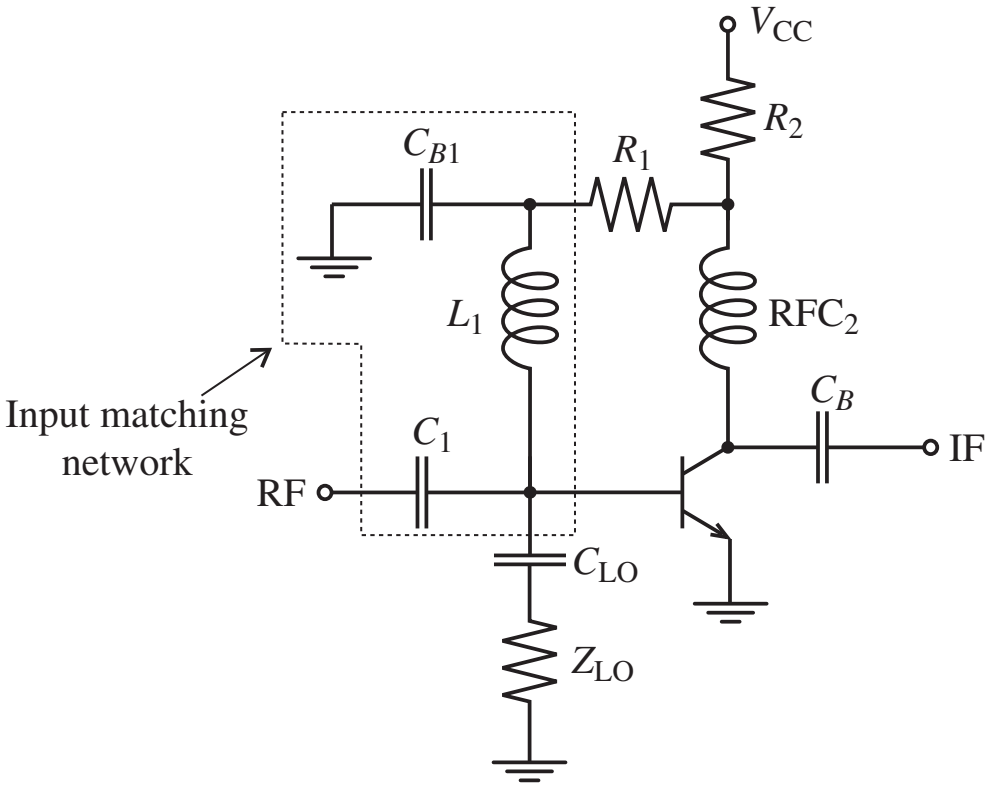


Figure 10-48 Modified input matching network.

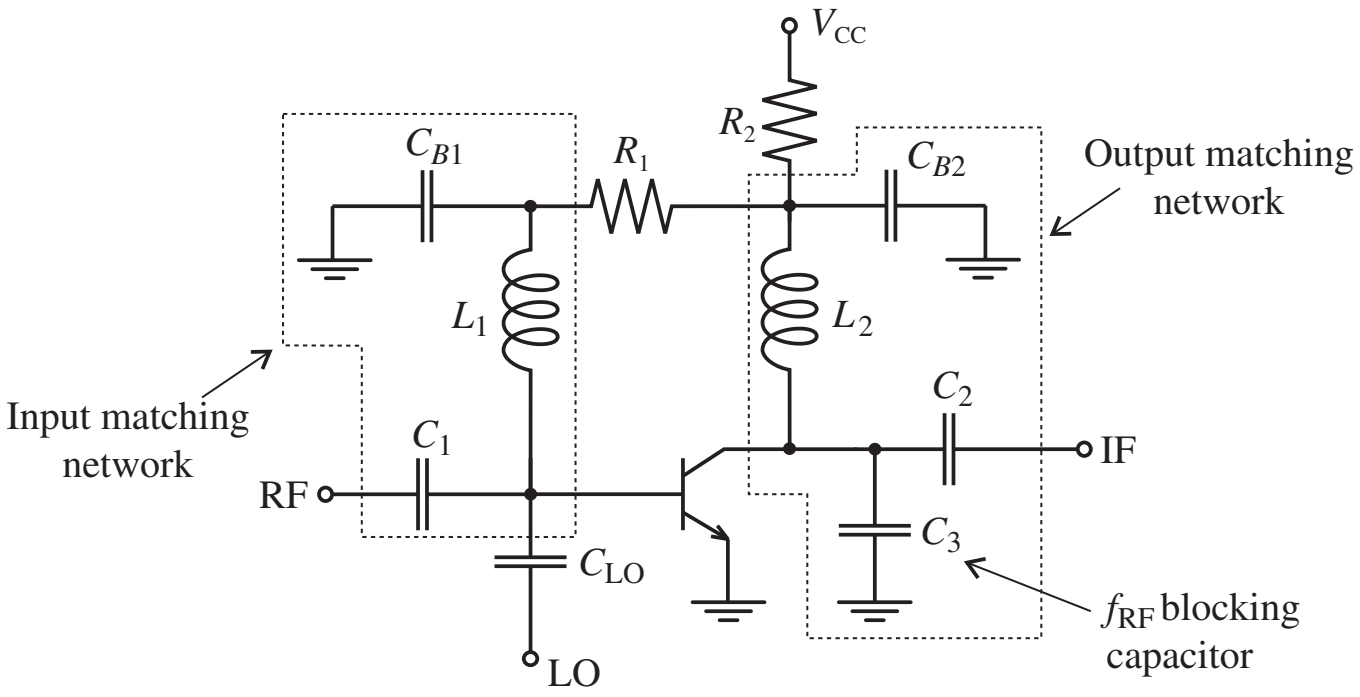


Figure 10-49 Complete electrical circuit of the low-side injection, single-ended BJT mixer with f_{RF} = 1900 MHz and f_{IF} = 200 MHz.

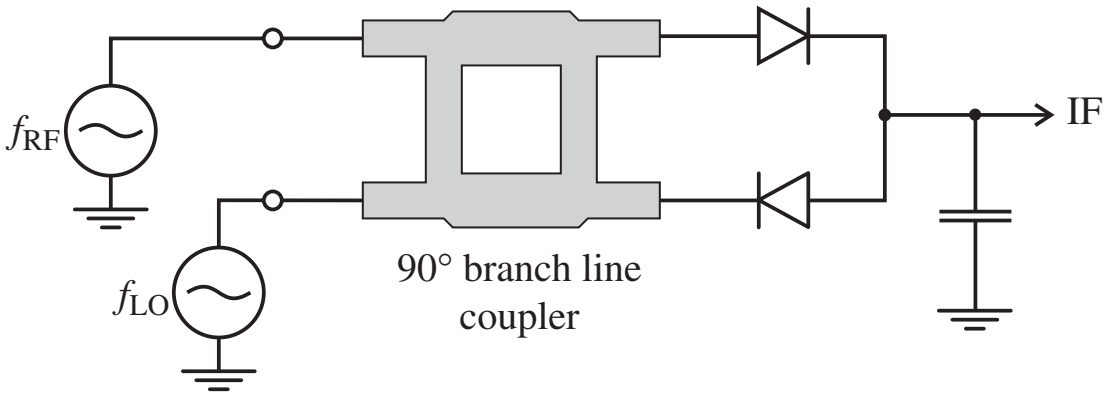


Figure 10-50 Balanced mixer involving a hybrid coupler.

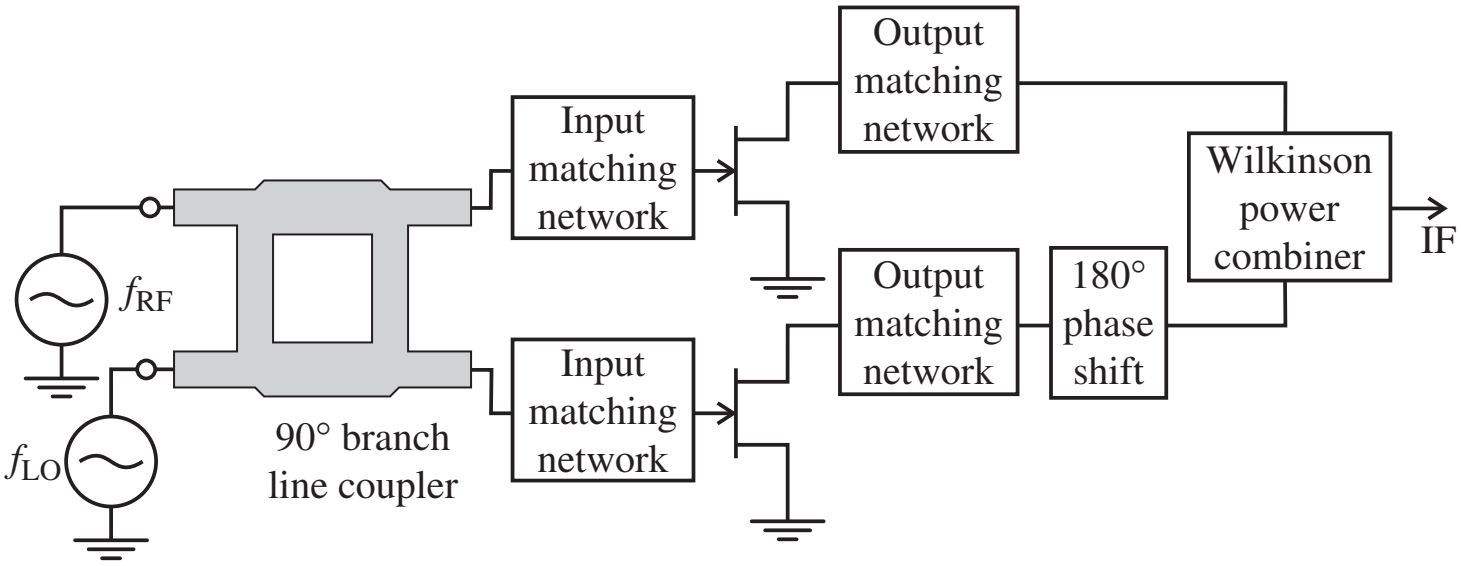


Figure 10-51 Single-balanced MESFET mixer with coupler and power combiner.

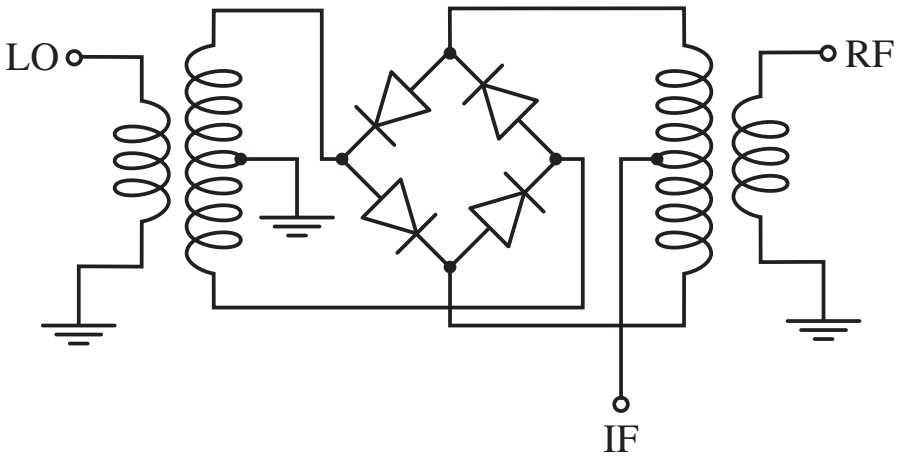


Figure 10-52 Double-balanced mixer design.

Table 10-3 Comparison of different active mixer topologies.

Mixer type	Advantages	Disadvantages
Active (vs. passive)	• Conversion gain • Better linearity • Lower LO power • Simpler to implement	• Typically higher noise figure • Less-predictable performance • Limited to lower frequencies
Unbalanced (active)	• Lowest noise figure • All ports single-ended	• Poor port-to-port isolation • Poor linearity • Difficult to implement
Single-balanced (active)	• LO-to-RF isolation • RF-to-IF isolation • Best linearity • Good noise figure	• Differential IF output • LO-to-IF feed-through
Double-balanced (active)	• LO-to-RF, LO-to-IF and RF-to-IF isolation • Good spurious product rejection • Good linearity • Simple to implement	• High noise figure • High power consumption

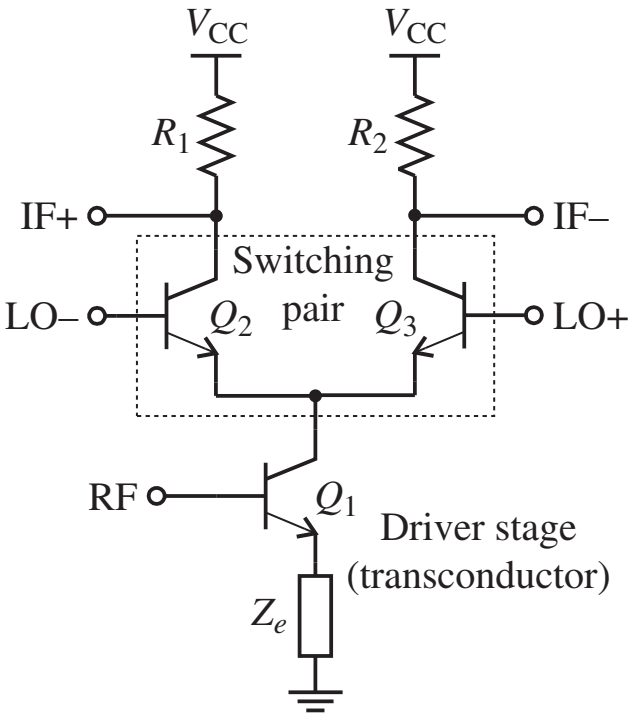


Figure 10-53 Single-balanced active mixer with drive stage.

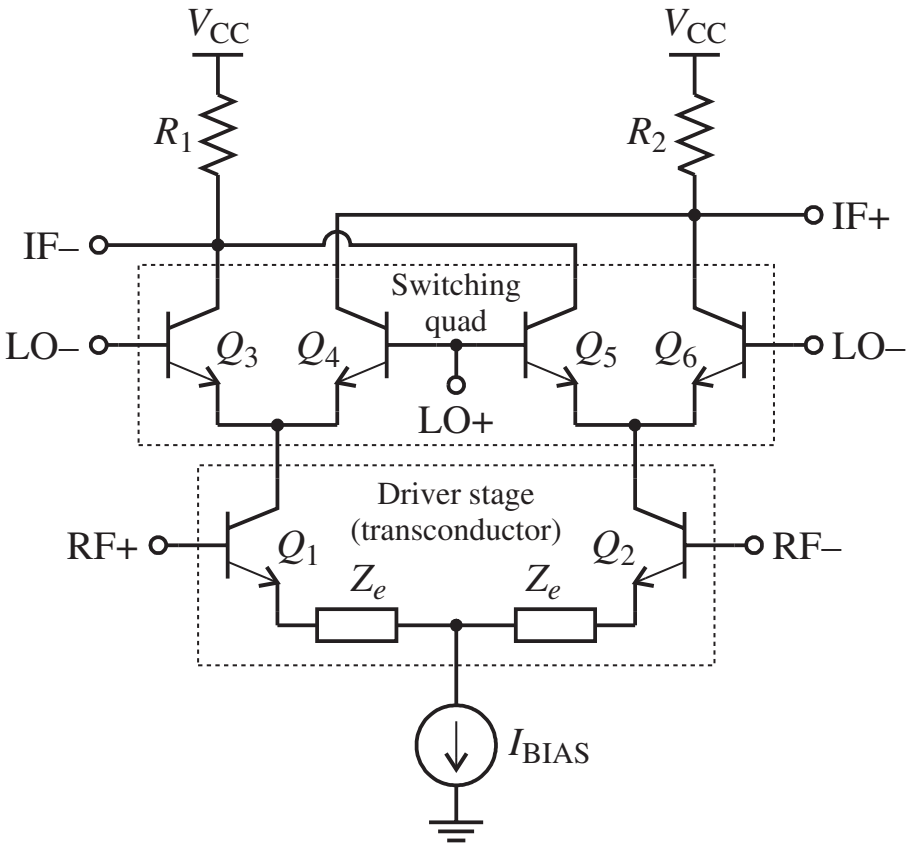


Figure 10-54 Double-balanced (Gilbert cell) active mixer.

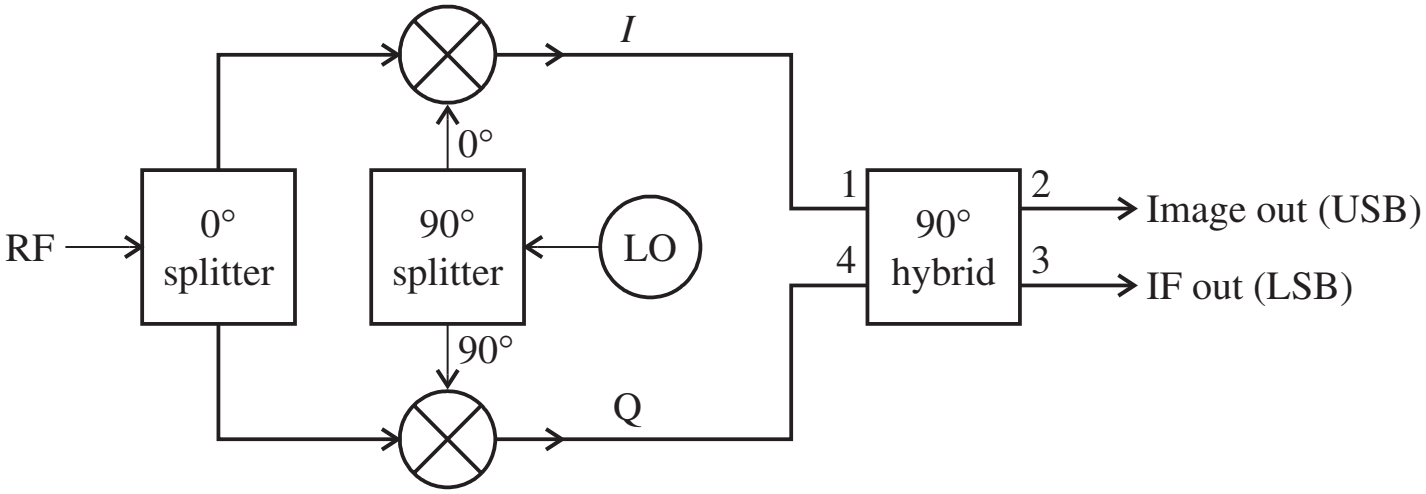


Figure 10-55 Image reject mixer.

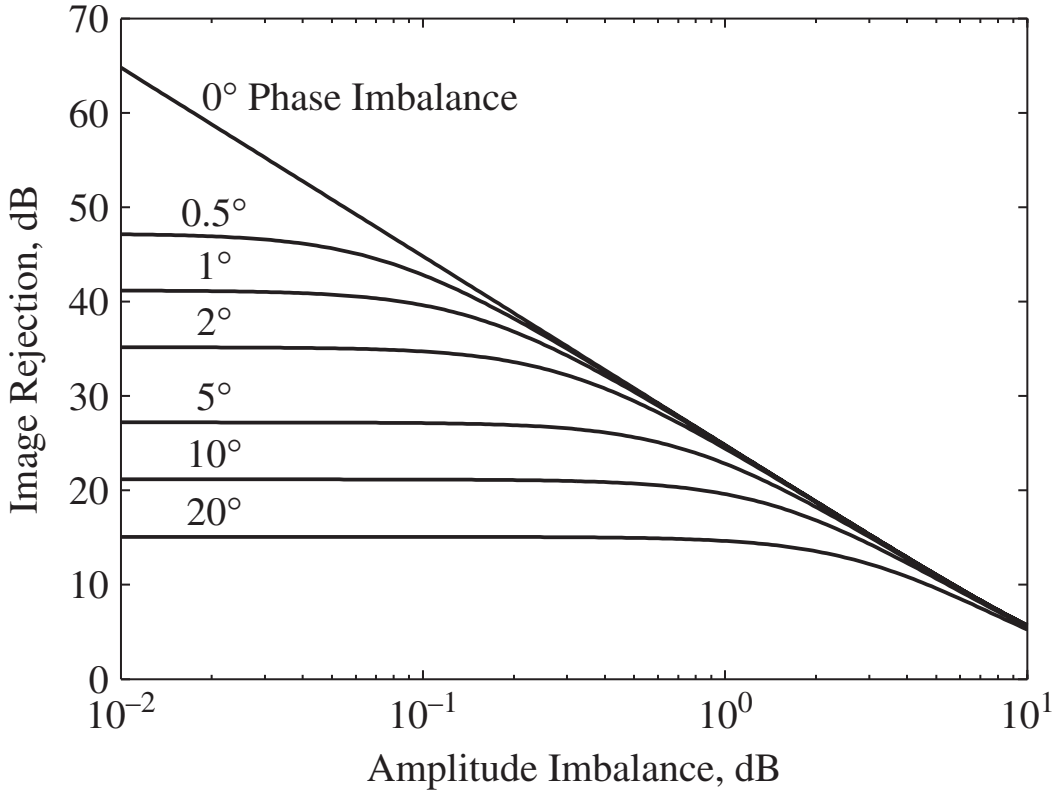


Figure 10-56 Image rejection as a function of amplitude and phase imbalance. Note the double logarithmic scale for amplitude imbalance (dB on a log scale).

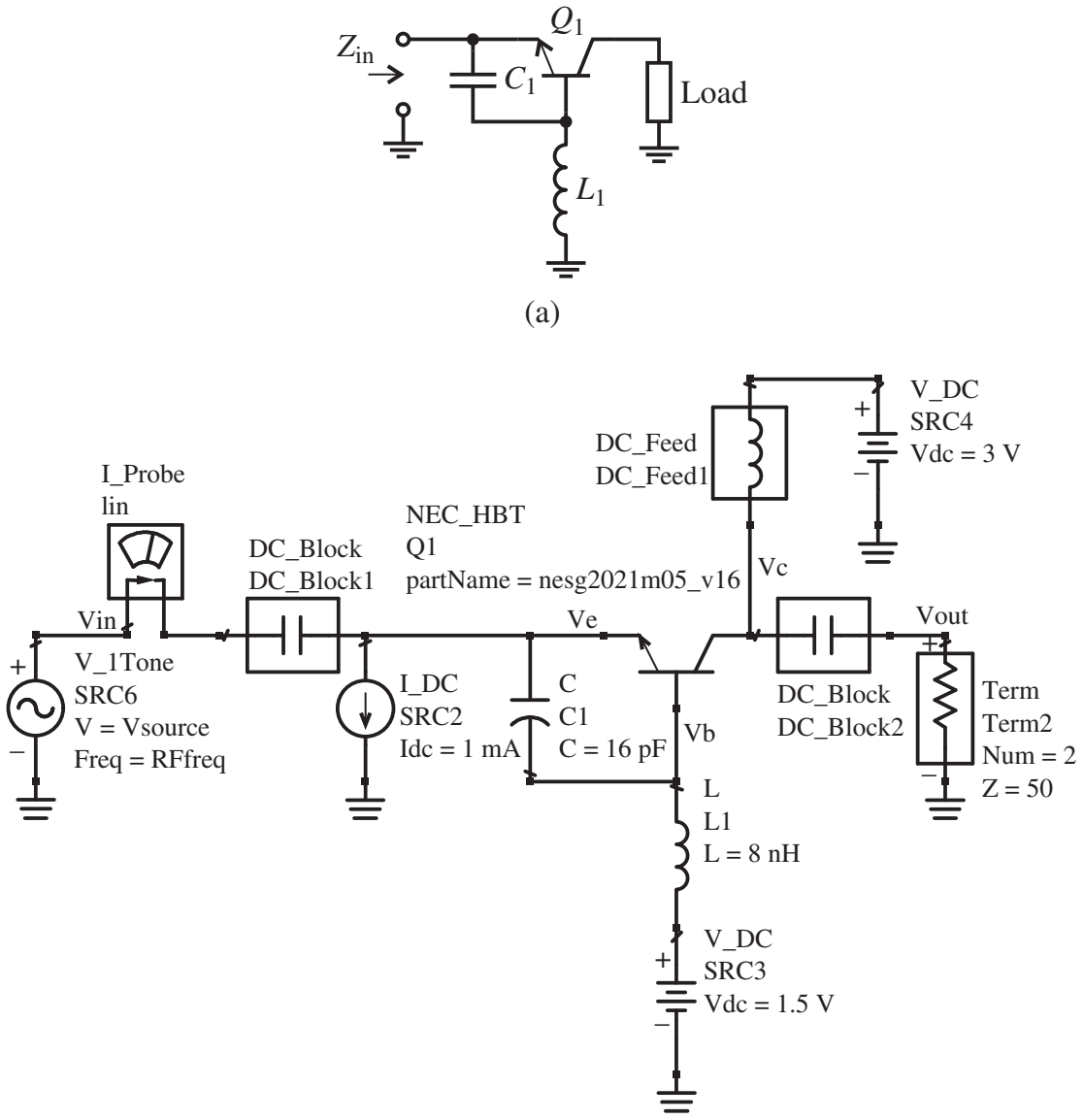


Figure 10-57 Base feedback negative resistance circuit:
(a) simplified, (b) with bias and excitation components for input impedance analysis.

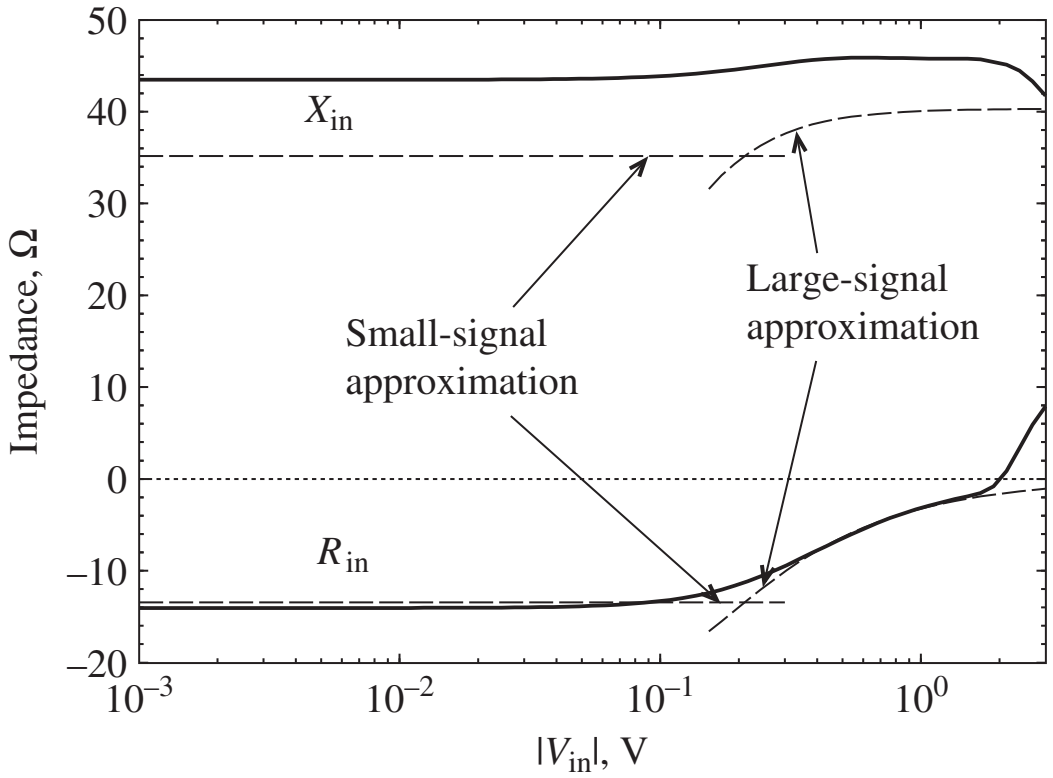


Figure 10-58 Harmonic balance simulation results for the example base feedback negative resistance circuit at 1 GHz.

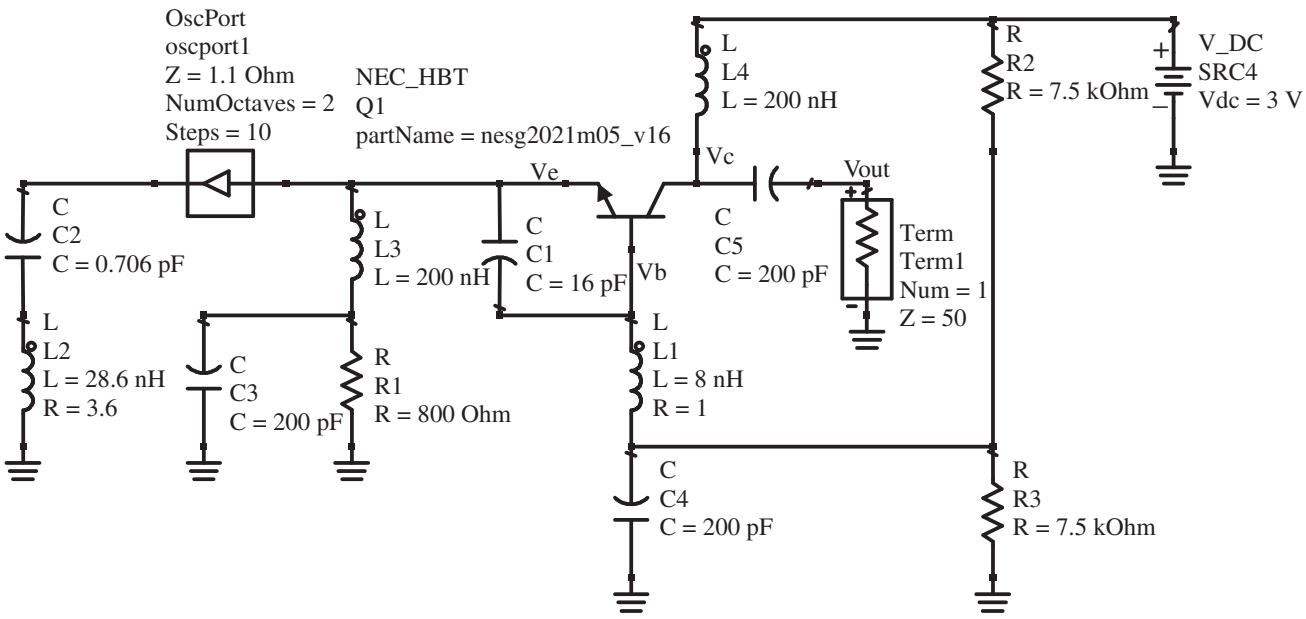


Figure 10-59 1 GHz oscillator utilizing base feedback and a series resonator.

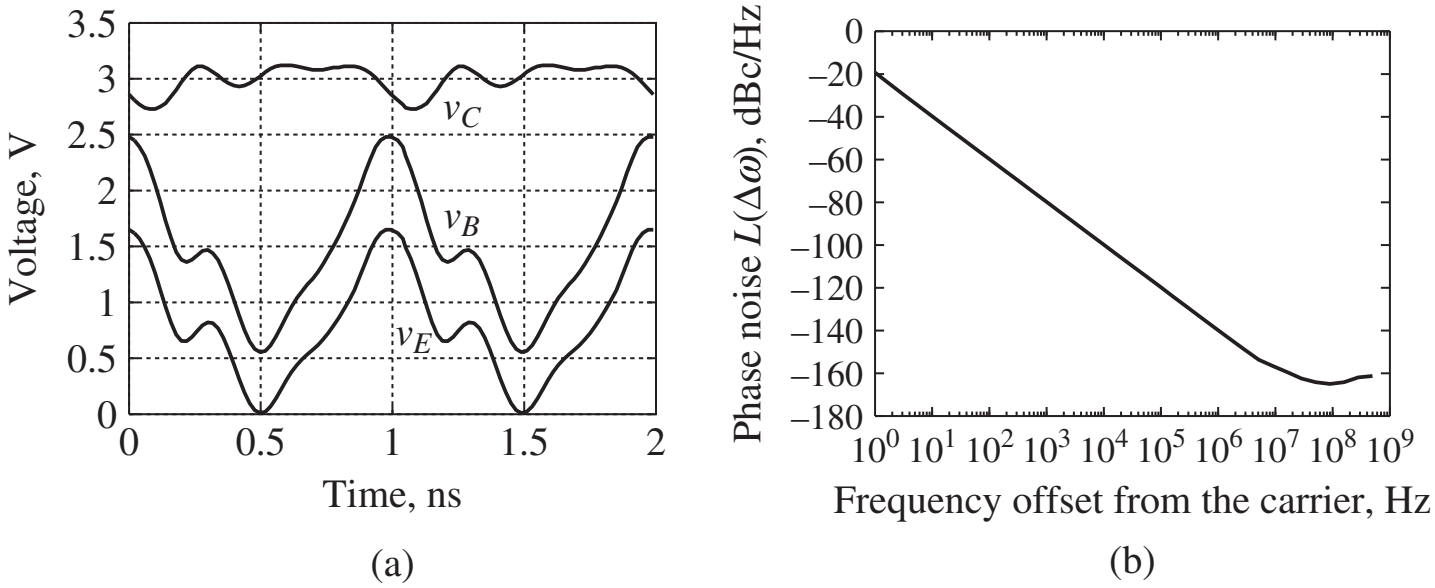


Figure 10-60 Harmonic balance simulation of the 1 GHz oscillator: (a) transistor voltage waveforms, (b) phase noise.

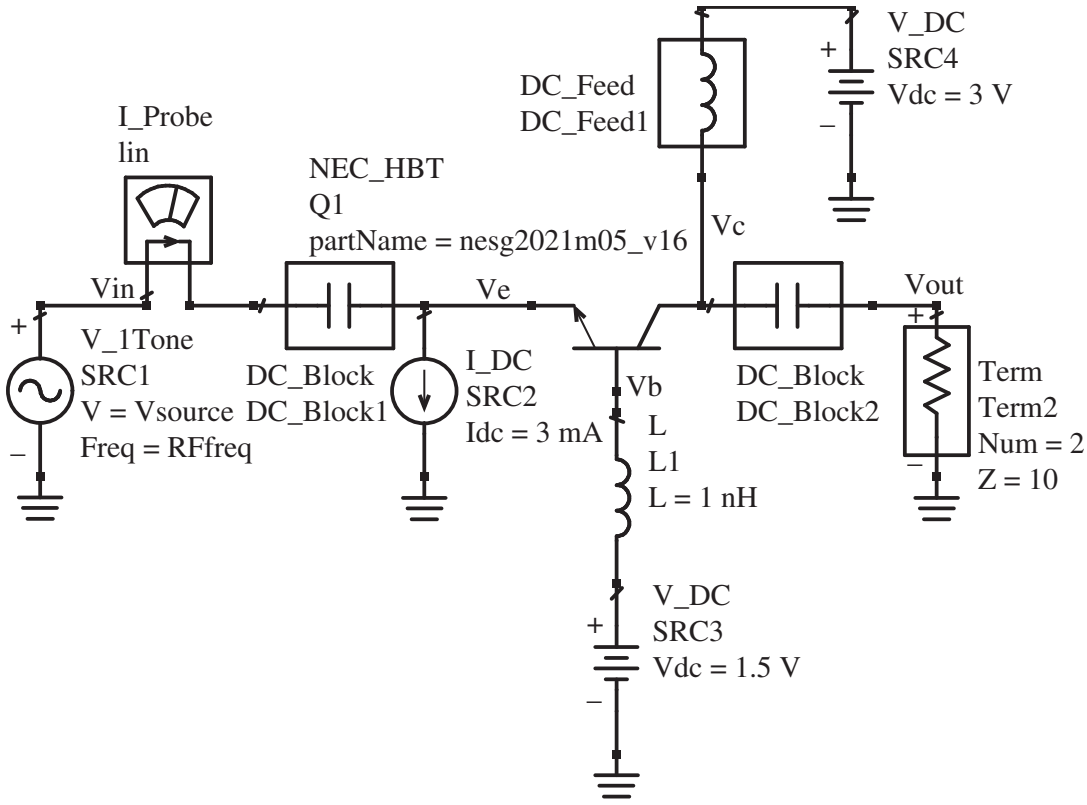


Figure 10-61 Simplified base feedback negative resistance circuit set up for input impedance analysis at 5 GHz.

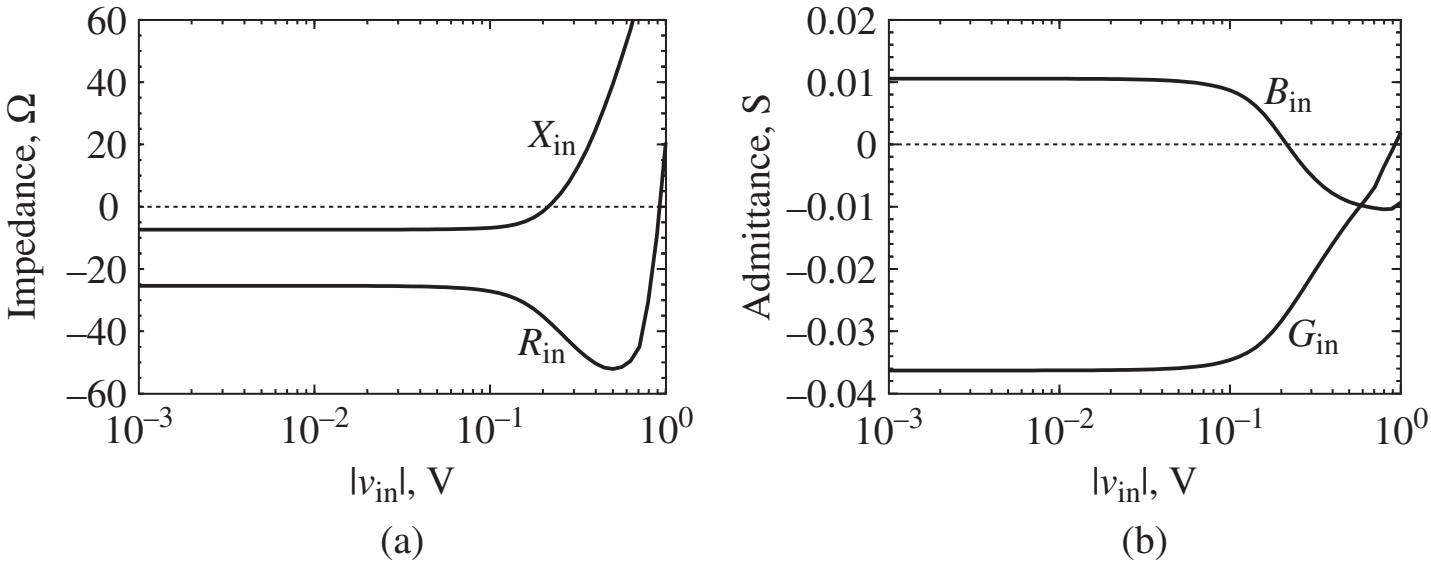


Figure 10-62 Harmonic balance simulation results for the simplified base feedback negative resistance circuit at 5 GHz: (a) input impedance, (b) input admittance.

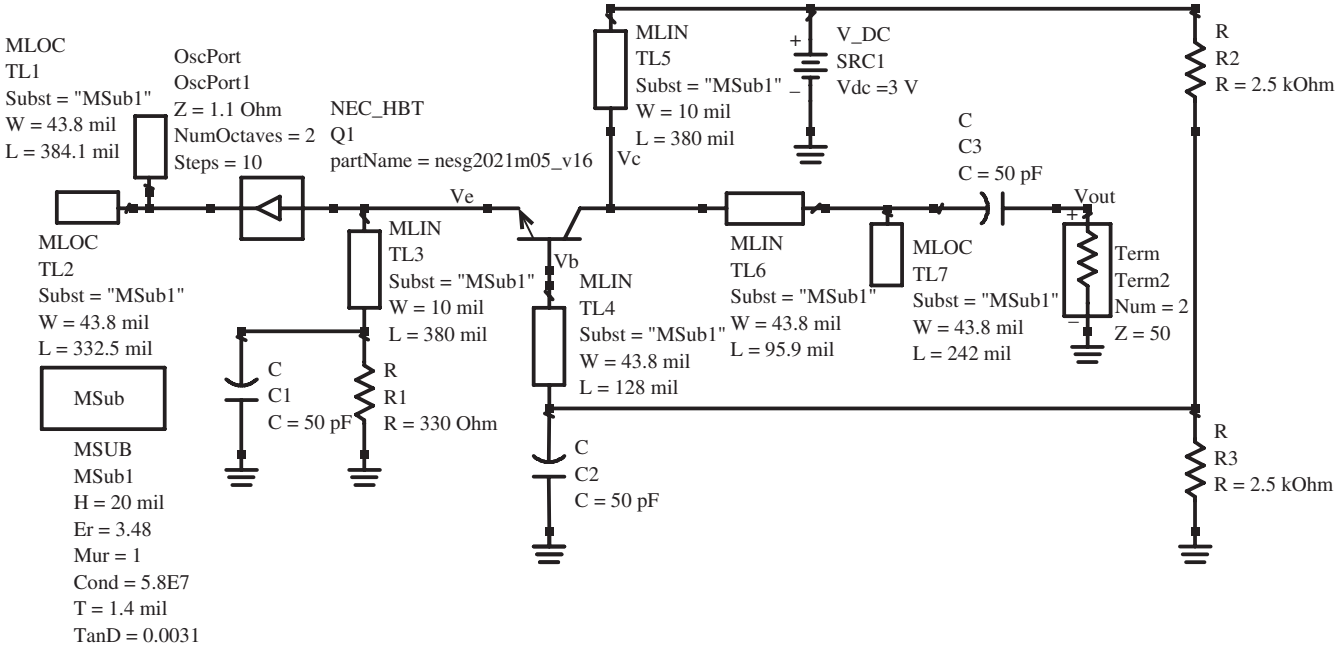


Figure 10-63 5 GHz oscillator utilizing base feedback and a parallel resonator.

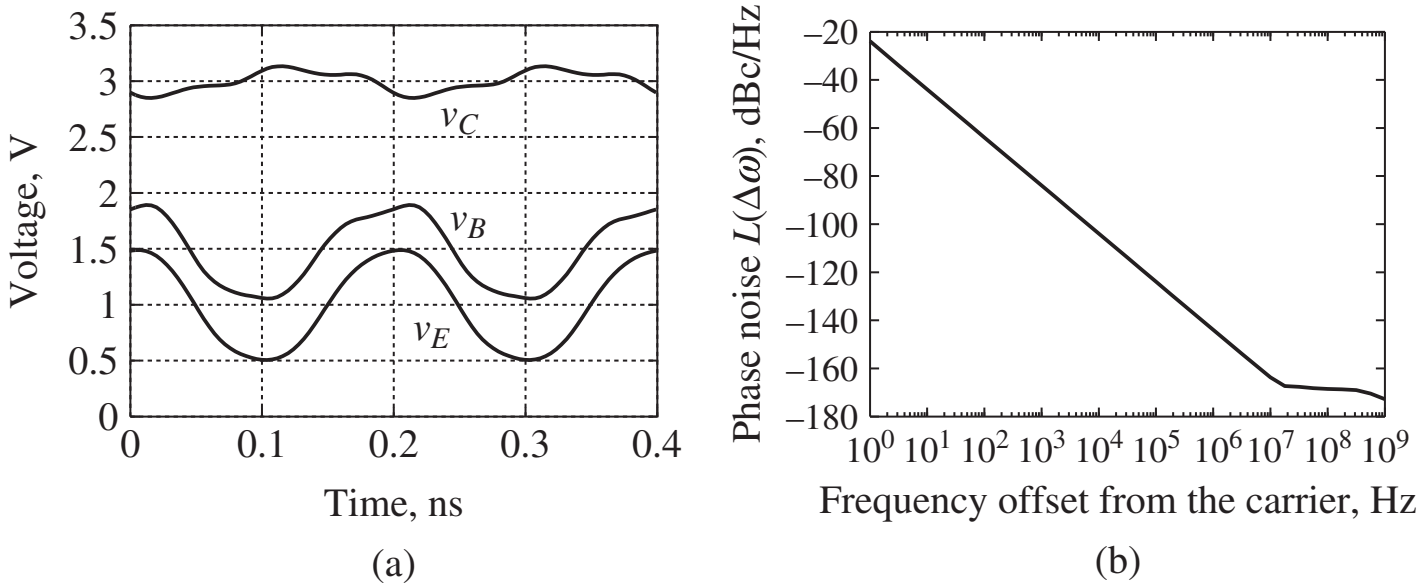


Figure 10-64 Harmonic balance simulation of the 5 GHz oscillator: (a) transistor voltage waveforms, (b) phase noise.