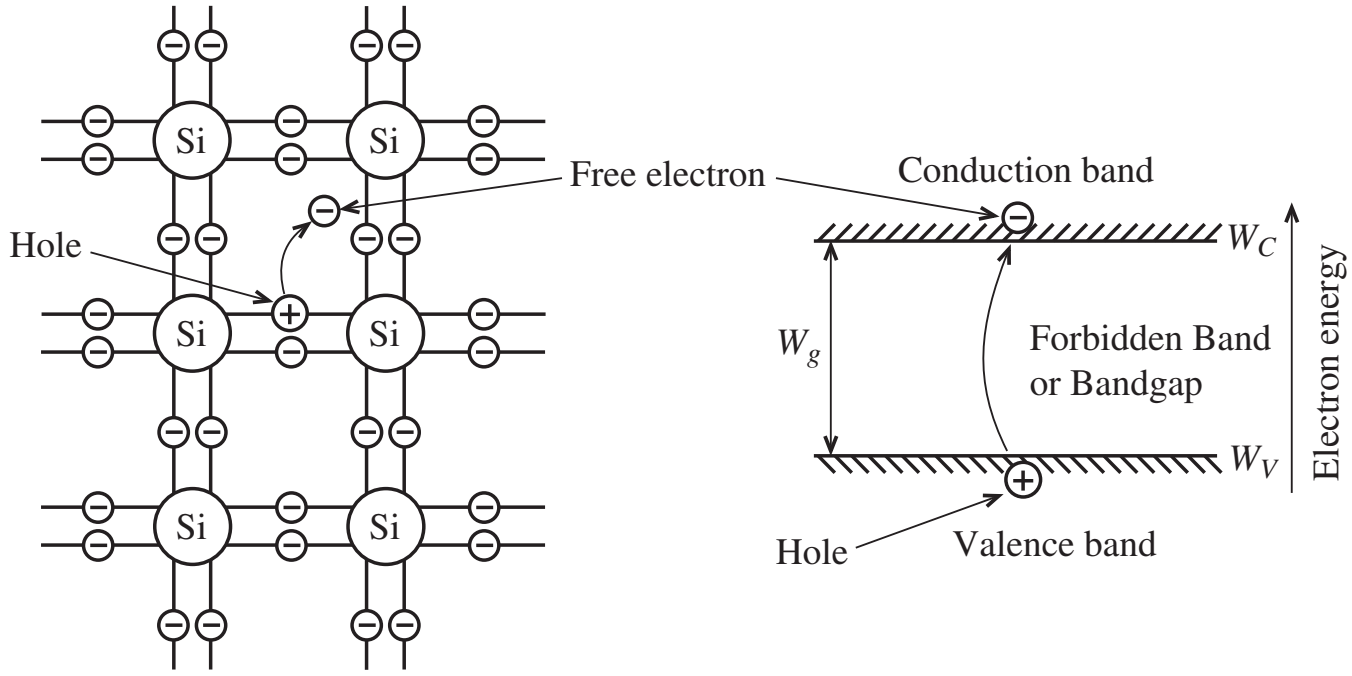
R. Ludwig and G. Bogdanov
"RF Circuit Design: Theory and Applications"
2nd edition

Figures for Chapter 6



(a) Planar representation of covalent bonds

(b) Energy band levels

Figure 6-1 Lattice structure and energy levels of silicon. (a) schematic planar crystal arrangement with thermal breakup of one valent bond resulting in a hole and a moving electron for $T > 0$ K. (b) equivalent energy band level representation whereby a hole is created in the valence band W_V and an electron is produced in the conduction band W_C. The energy gap between both bands is indicated by W_g.

Table 6-1 Effective concentrations and effective mass values at T = 300 K

Semiconductor	m_n^*/m_0	m_p^*/m_0	N_C, cm^{-3}	N_V, cm^{-3}	n_i, cm^{-3}
Silicon (Si)	1.08	0.56	2.8×10^{19}	1.04×10^{19}	1.45×10^{10}
Germanium (Ge)	0.55	0.37	1.04×10^{19}	6.0×10^{18}	2.4×10^{13}
Gallium Arsenide (GaAs)	0.067	0.48	4.7×10^{17}	7.0×10^{18}	1.79×10^{6}

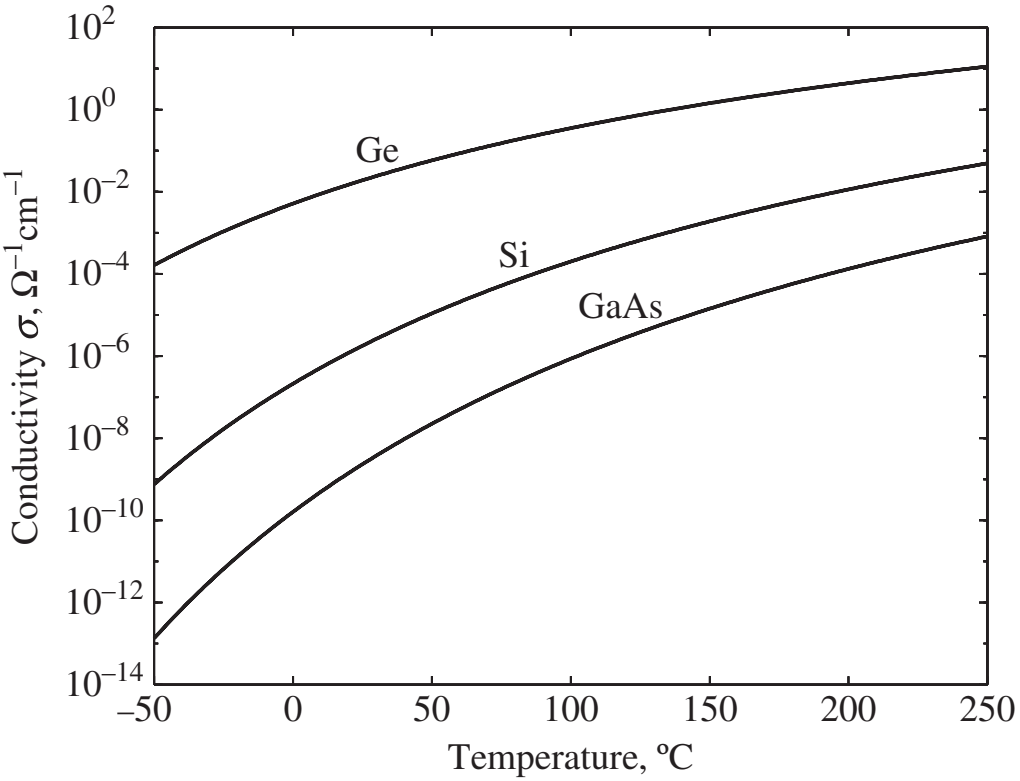


Figure 6-2 Conductivity of Si, Ge, GaAs in the range from –50℃ to 250℃.

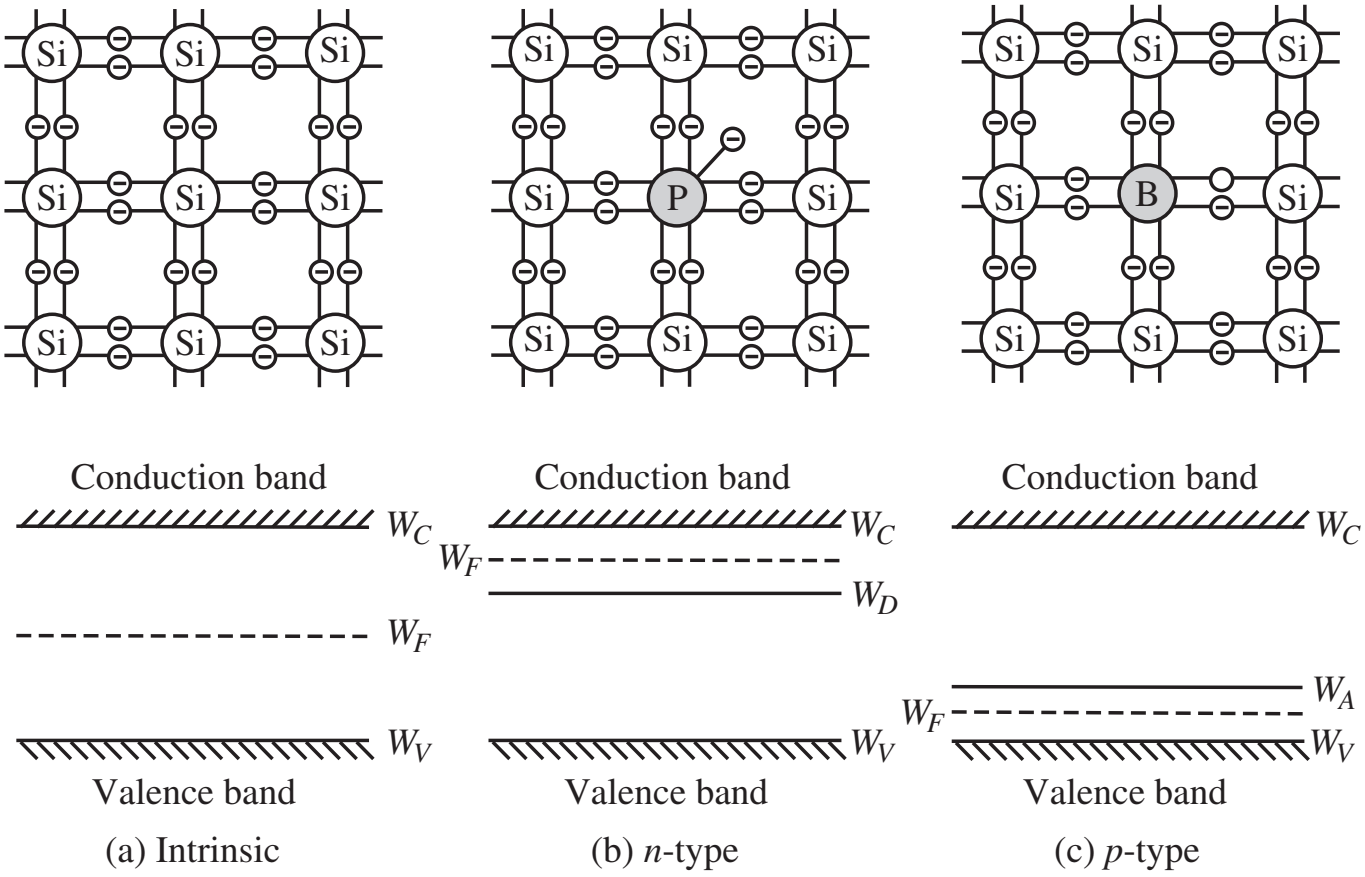


Figure 6-3 Lattice structure and energy band model for (a) intrinsic, (b) *n*-type, and (c) *p*-type semiconductors at no thermal energy. W_D and W_A are donor and acceptor energy levels.

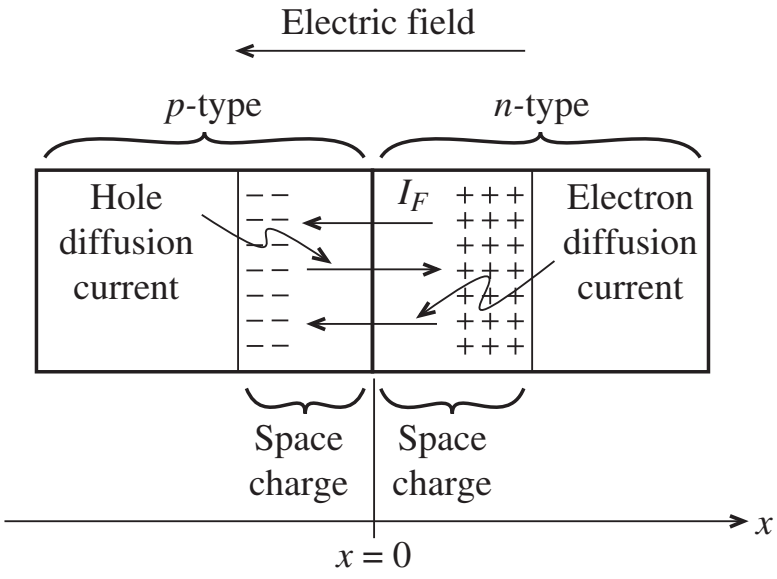
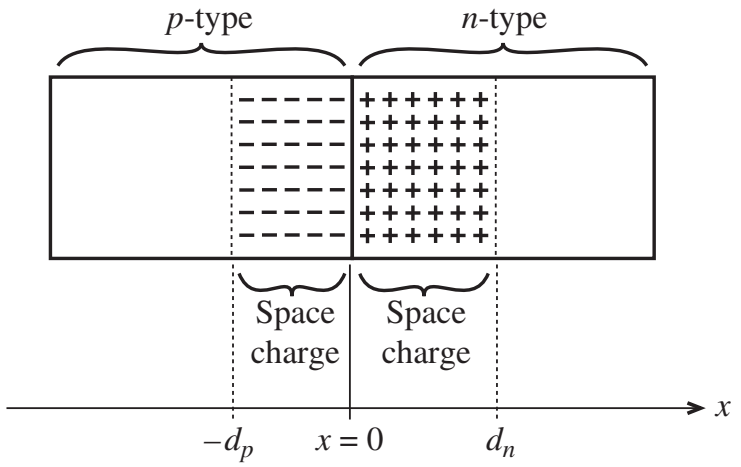
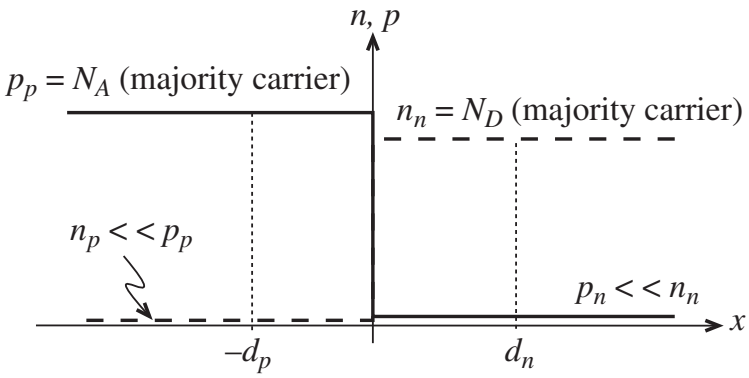


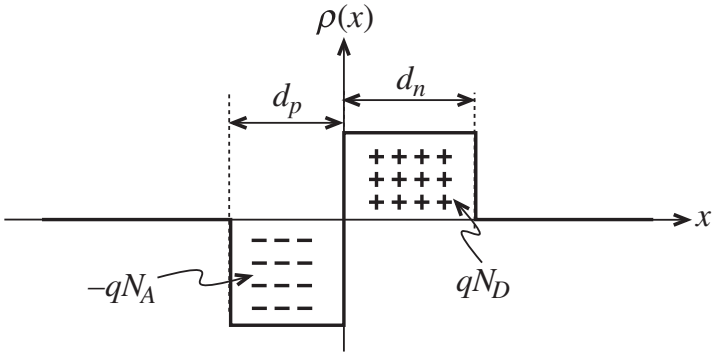
Figure 6-4 Current flows in the *pn*-junction.



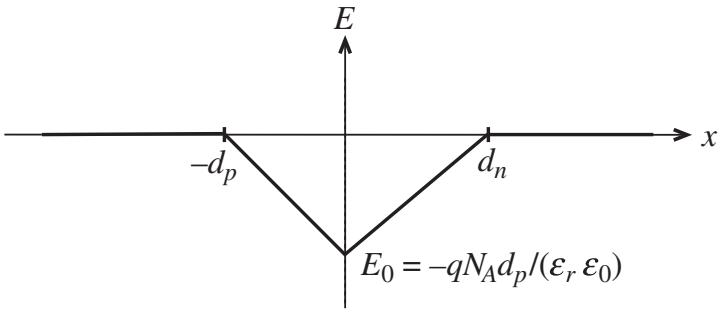
(a) *pn*-junction with space charge extent



(b) Acceptor and donor concentrations

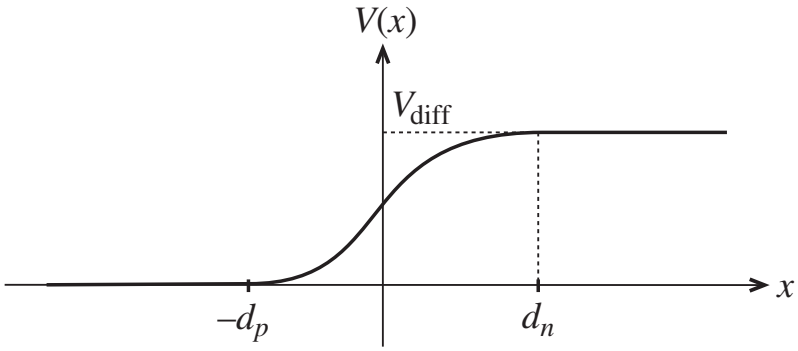


(c) Polarity of charge density distribution



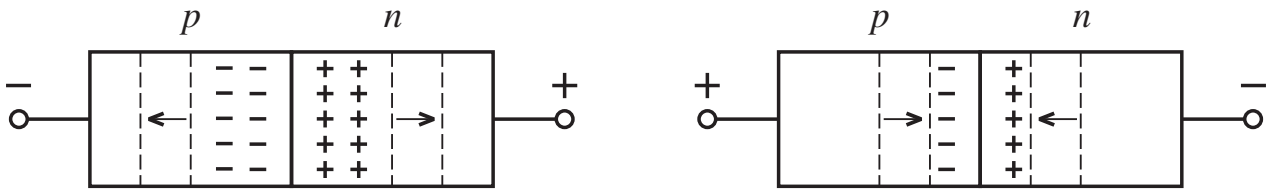
(d) Electric field distribution

Figure 6-5 The *pn*-junction with abrupt charge carrier transition in the absence of an externally applied voltage.

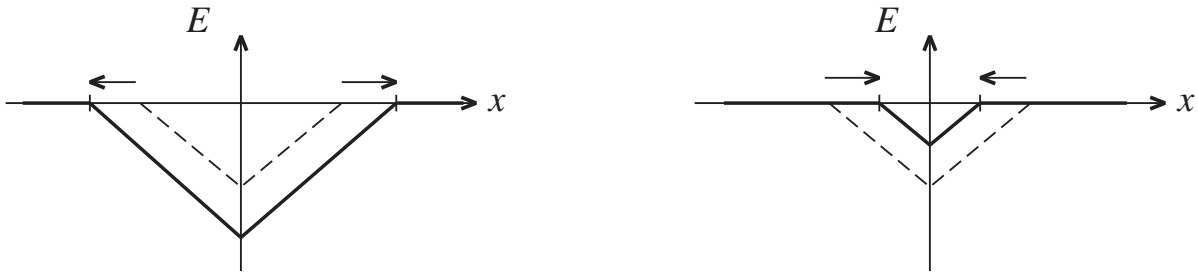


(e) Barrier voltage distribution

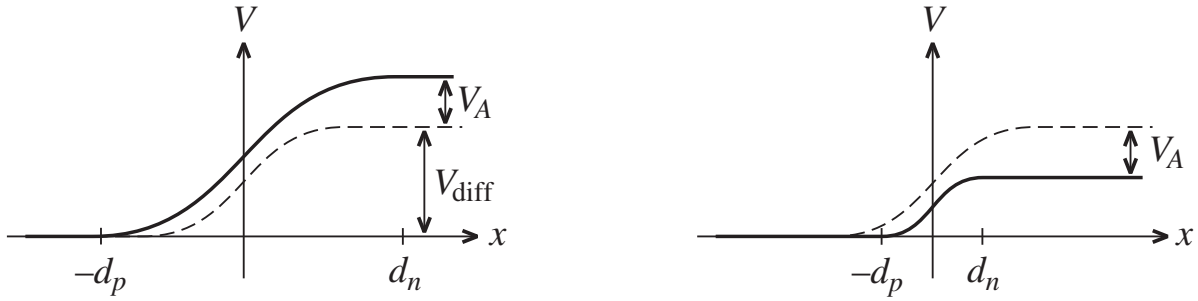
Figure 6-5 The *pn*-junction with abrupt charge carrier transition in the absence of an externally applied voltage. (Continued)



Space charge distribution in the *pn*-junction



Electric field distribution in the *pn*-junction



Voltage distribution in the *pn*-junction

(a) Reverse biasing ($V_A < 0$) (b) Forward biasing ($V_A > 0$)

Figure 6-6 External voltage applied to the *pn*-junction in reverse and forward directions.

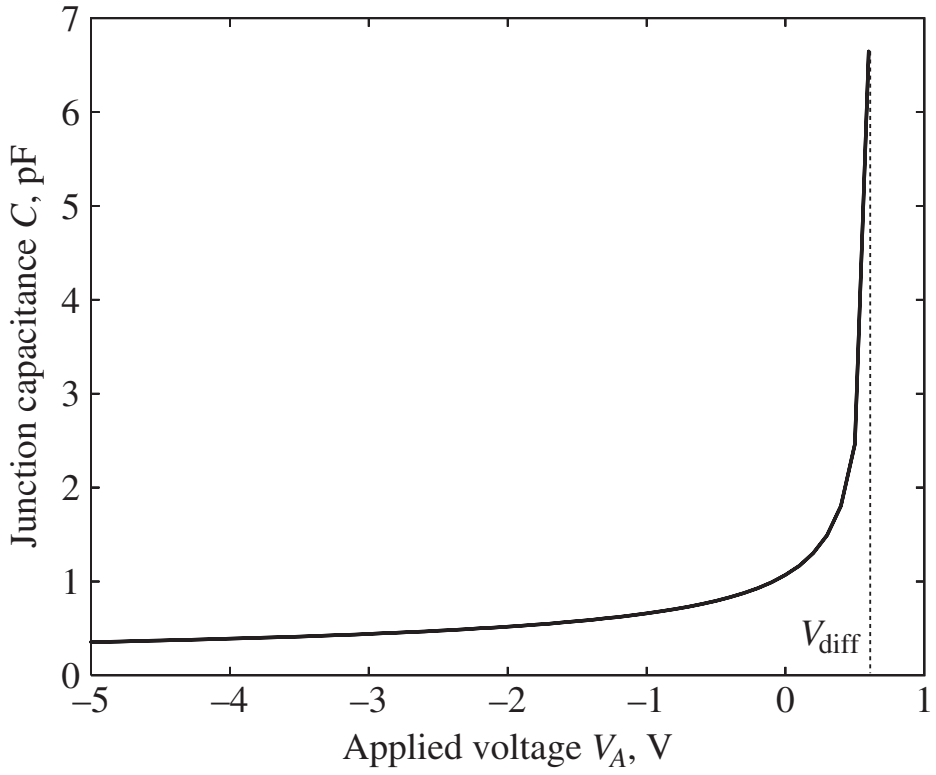


Figure 6-7 The *pn*-junction capacitance as a function of applied voltage.

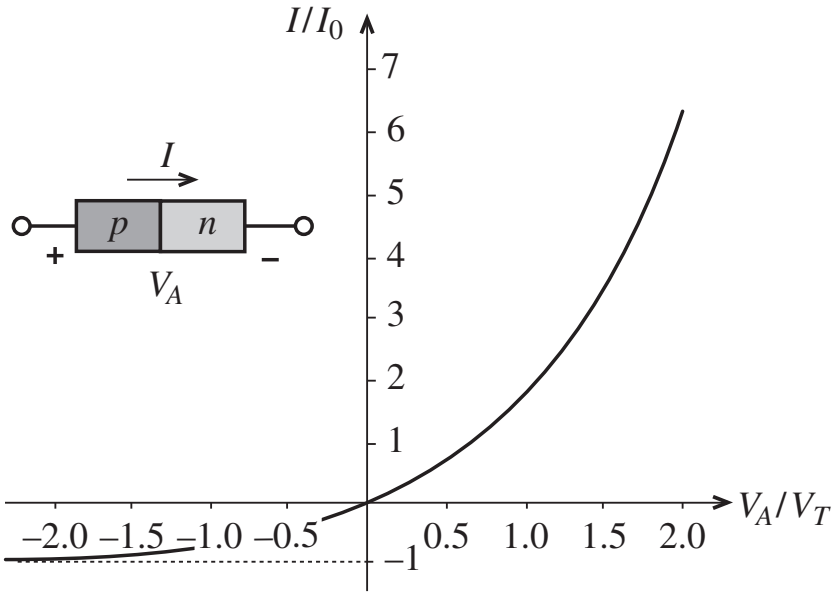
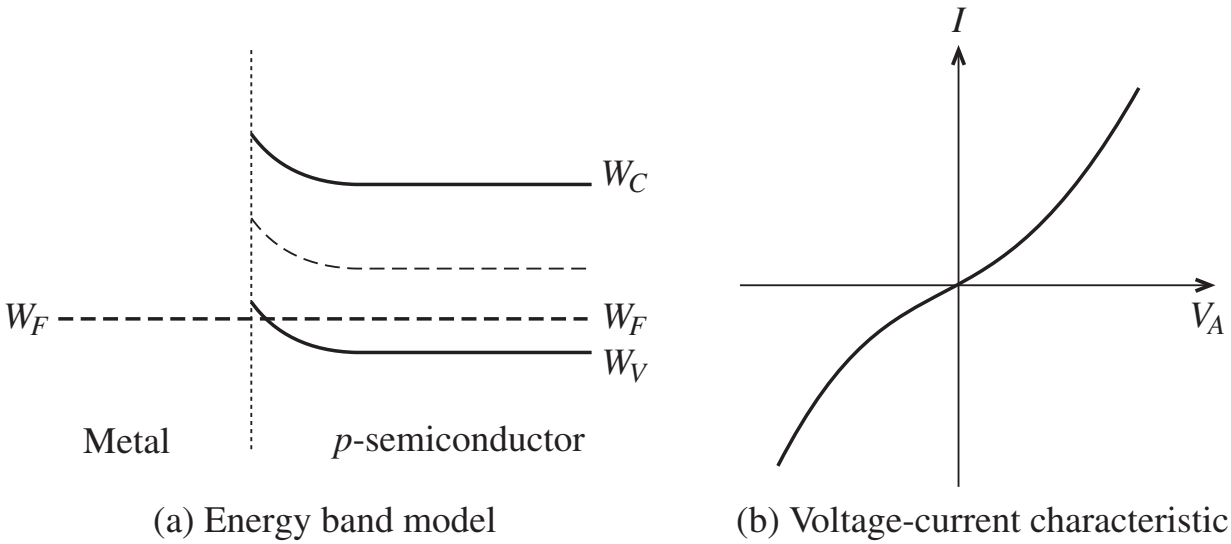


Figure 6-8 Current-voltage behavior of *pn*-junction based on Shockley equation.



(a) Energy band model (b) Voltage-current characteristic

Figure 6-9 Metal electrode in contact with *p*-semiconductor.

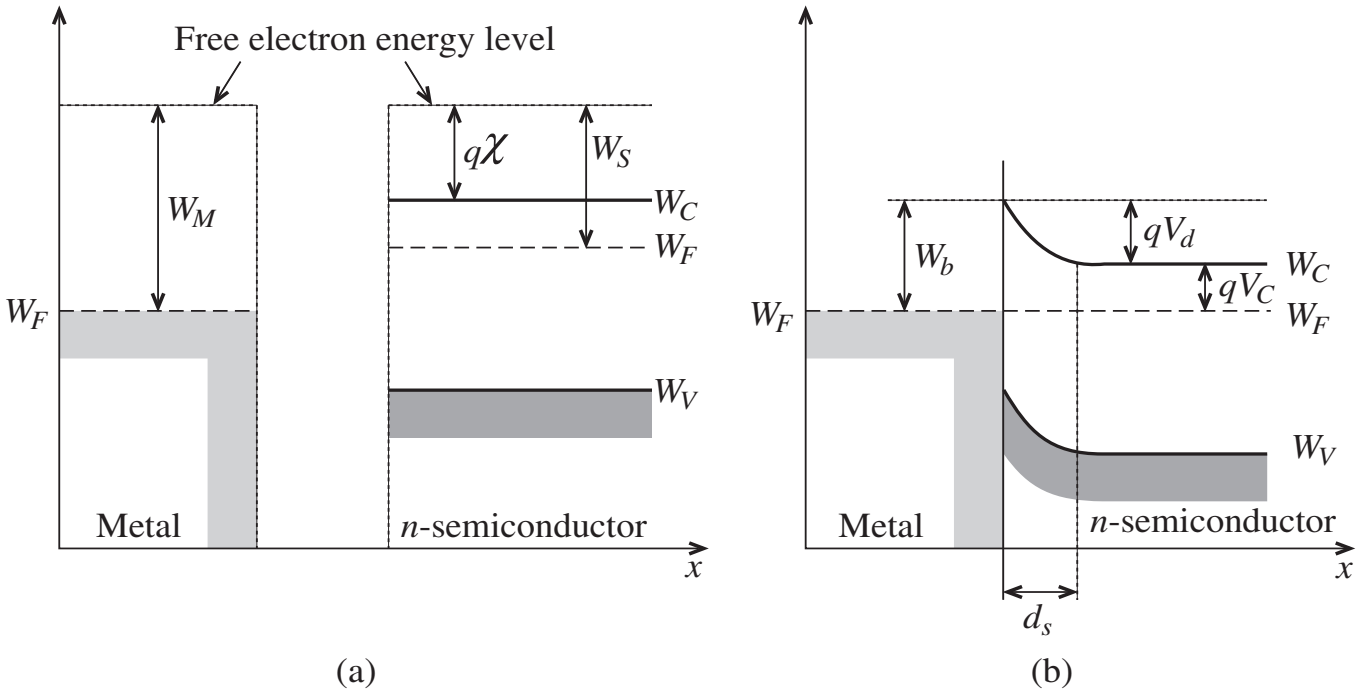


Figure 6-10 Energy band diagram of Schottky contact, (a) before and (b) after contact.

Table 6-2 Work function potentials of some metals

Material	Work Function Potential, V_M
Silver (Ag)	4.26 V
Aluminum (Al)	4.28 V
Gold (Au)	5.10 V
Chromium (Cr)	4.50 V
Molybdenum (Mo)	4.60 V
Nickel (Ni)	5.15 V
Palladium (Pd)	5.12 V
Platinum (Pt)	5.65 V
Titanium (Ti)	4.33 V

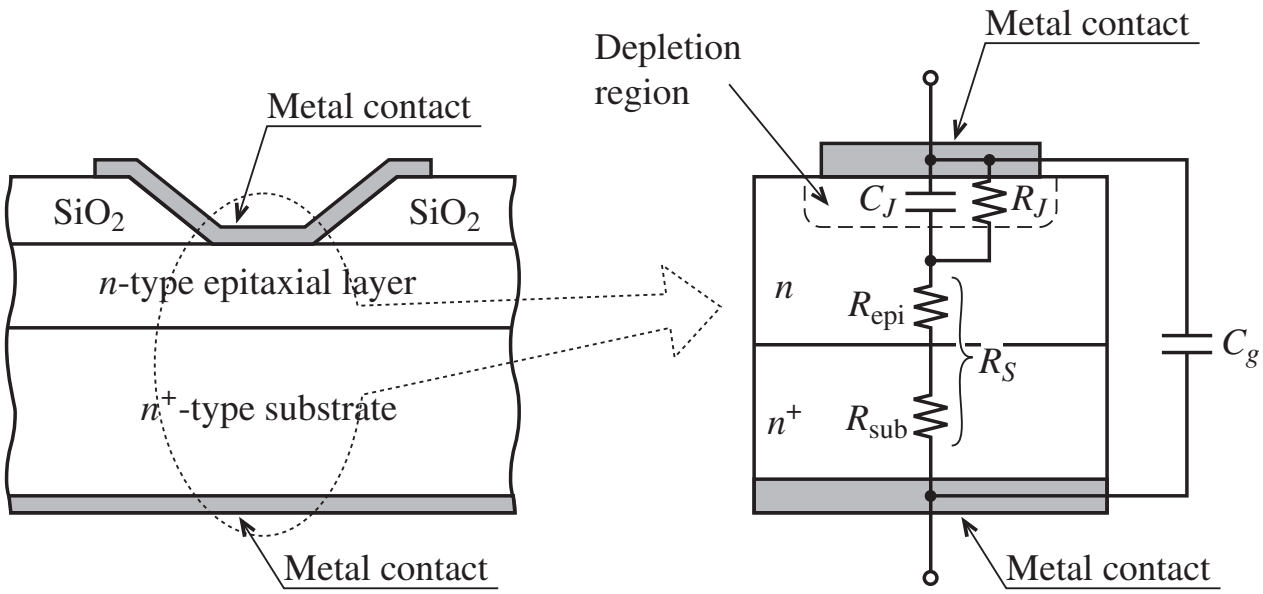


Figure 6-11 Cross-sectional view of Si Schottky diode.

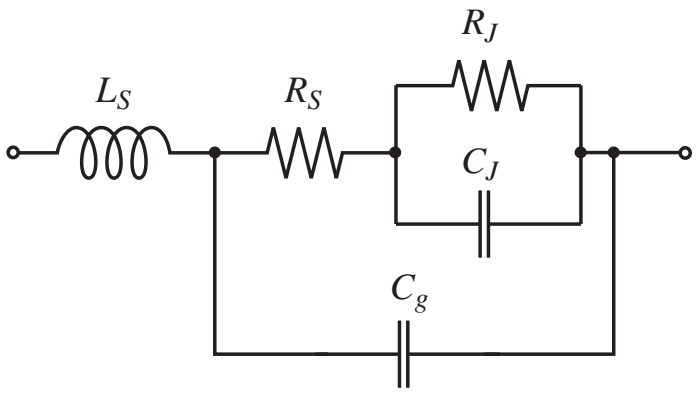


Figure 6-12 Circuit model of typical Schottky diode under forward bias.

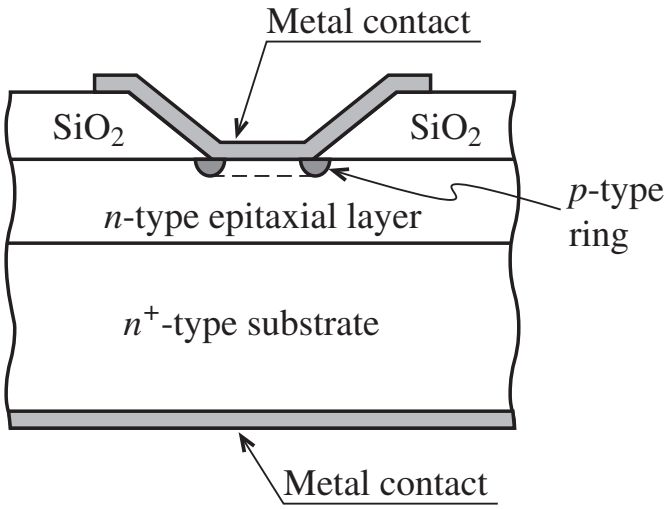
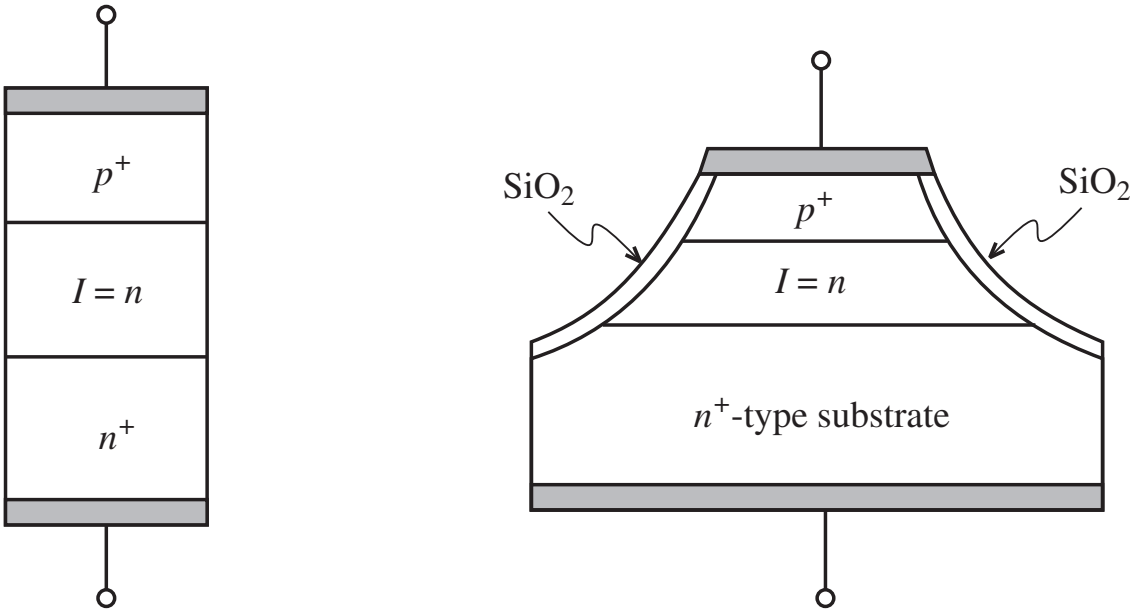


Figure 6-13 Schottky diode with additional isolation ring suitable for very high frequency applications.



(a) Simplified structure of a PIN diode (b) Fabrication in mesa processing technology

Figure 6-14 PIN diode construction.

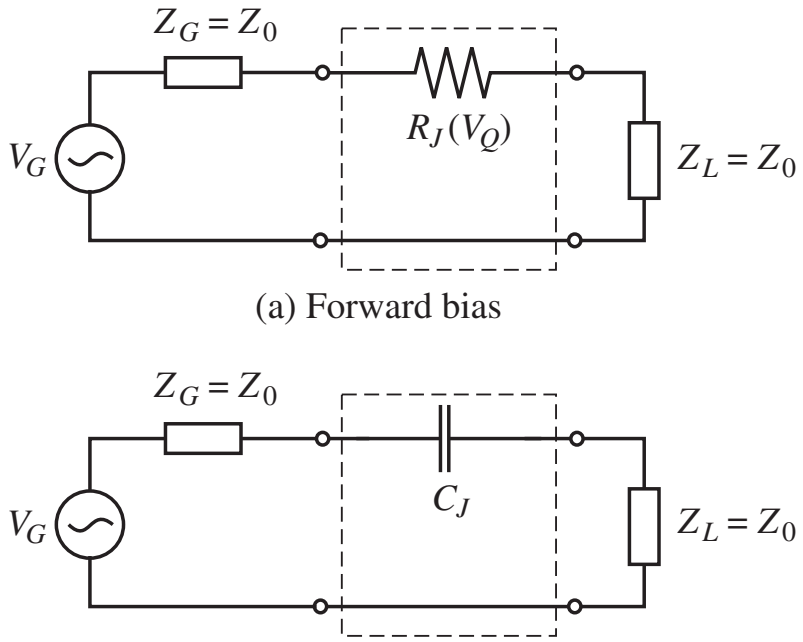
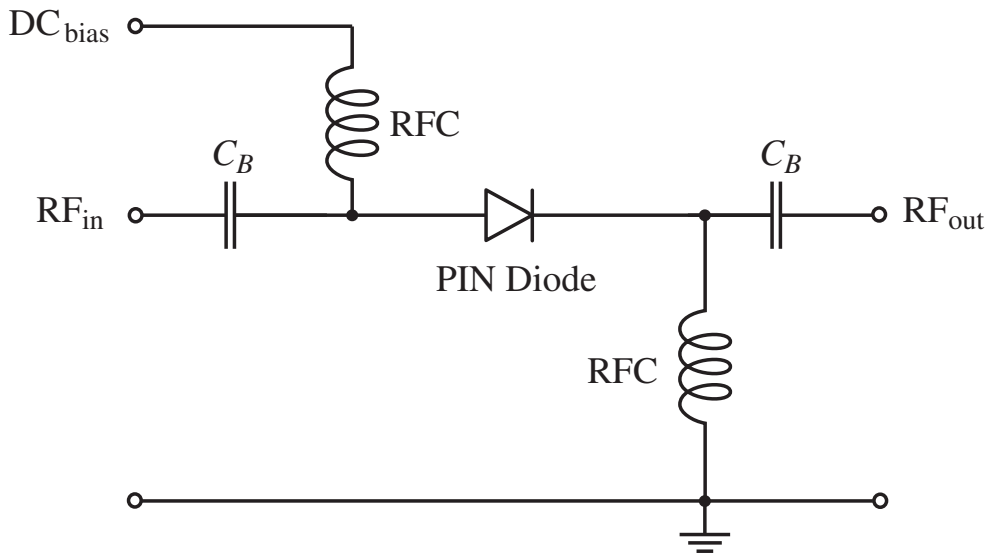
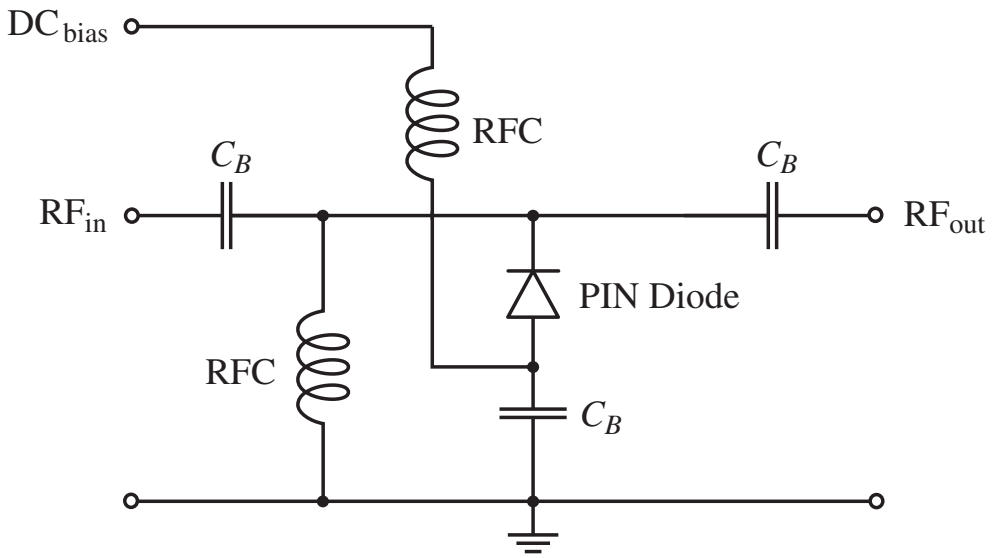


Figure 6-15 PIN diode in series connection.



(a) Series connection of PIN diode



(b) Shunt connection of PIN diode

Figure 6-16 Attenuator circuit with biased PIN diode in series and shunt configurations.

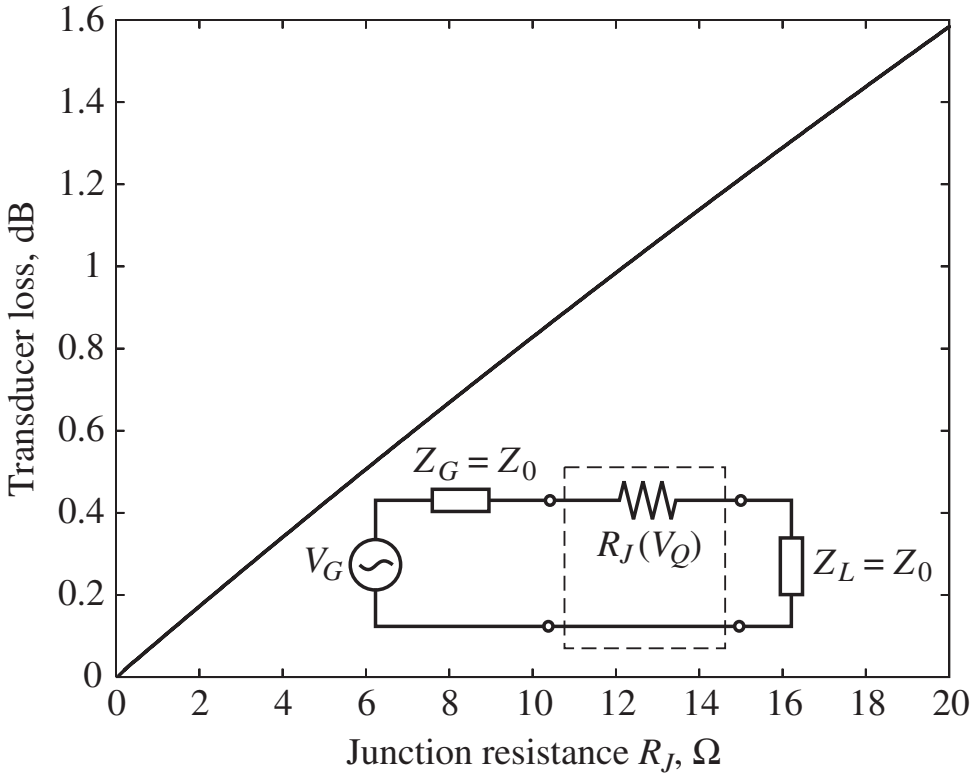


Figure 6-17 Transducer loss of series connected PIN diode under forward-bias condition. The diode behaves as a resistor.

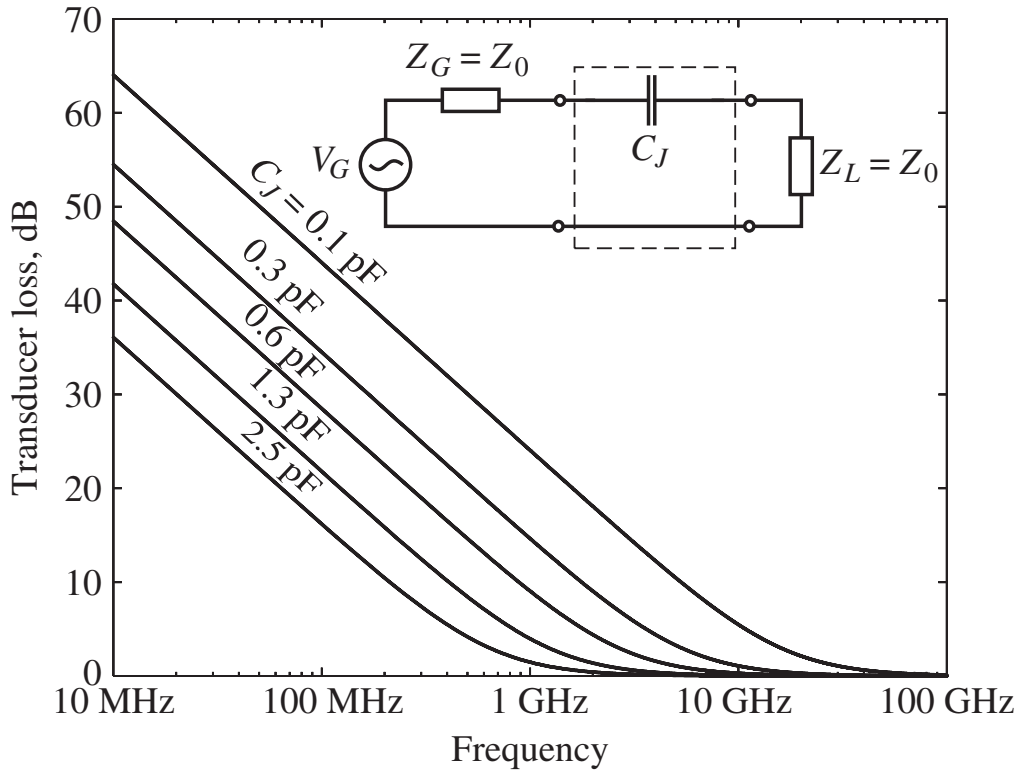


Figure 6-18 Transducer loss of series connected PIN diode under reverse-bias condition. The diode behaves as a capacitor.

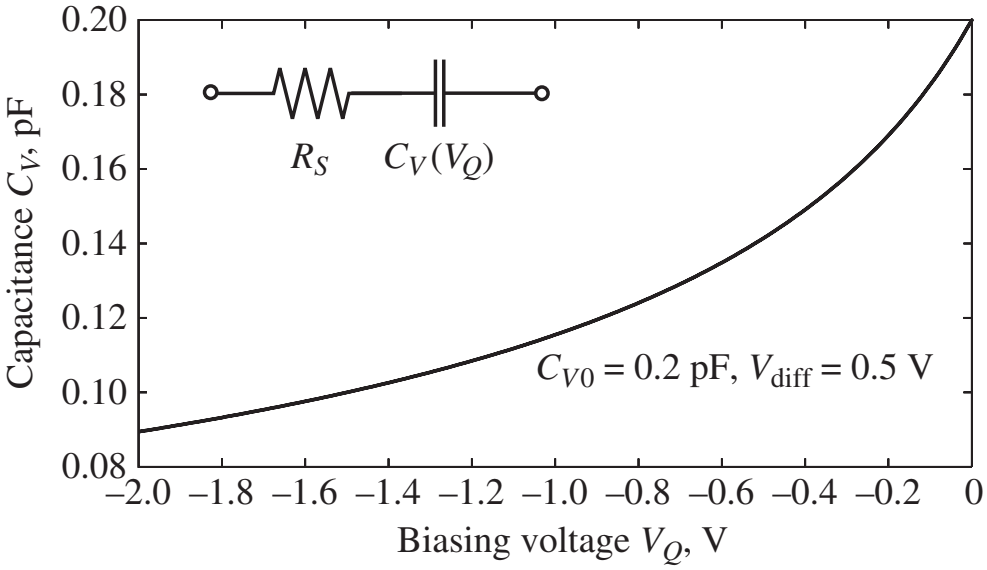


Figure 6-19 Simplified electric circuit model and capacitance behavior of varactor diode.

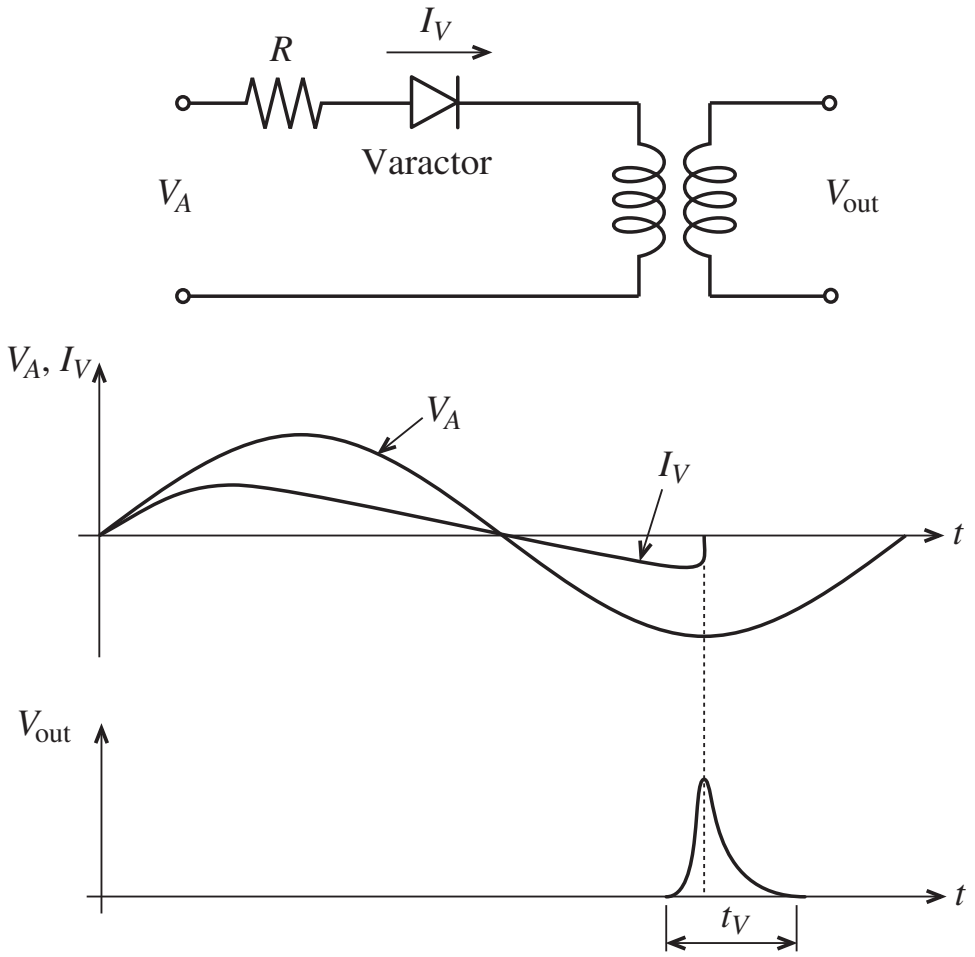
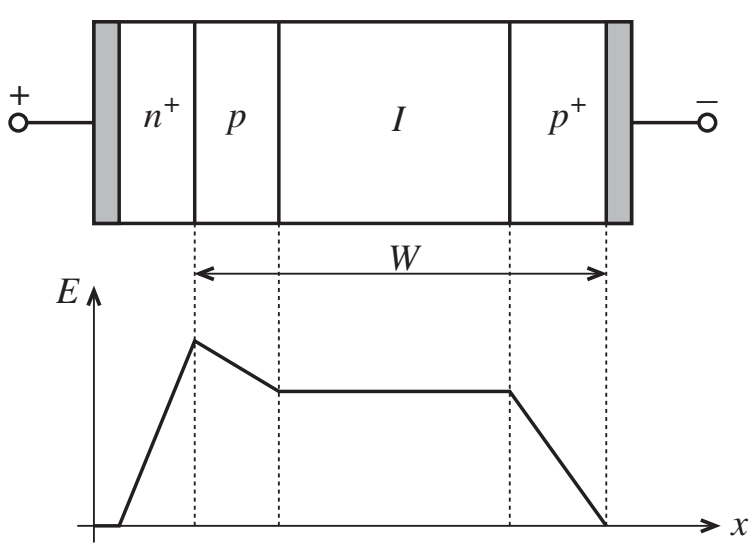
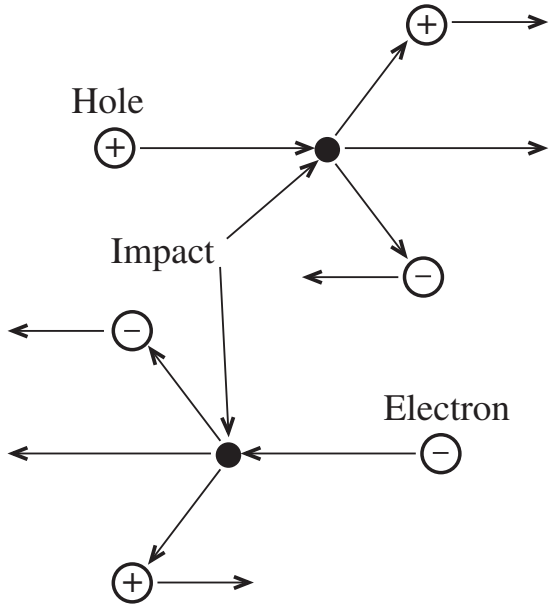


Figure 6-20 Pulse generation with a varactor diode.



(a) Layer structure and electric field profile



(b) Impact ionization

Figure 6-21 IMPATT diode behavior.

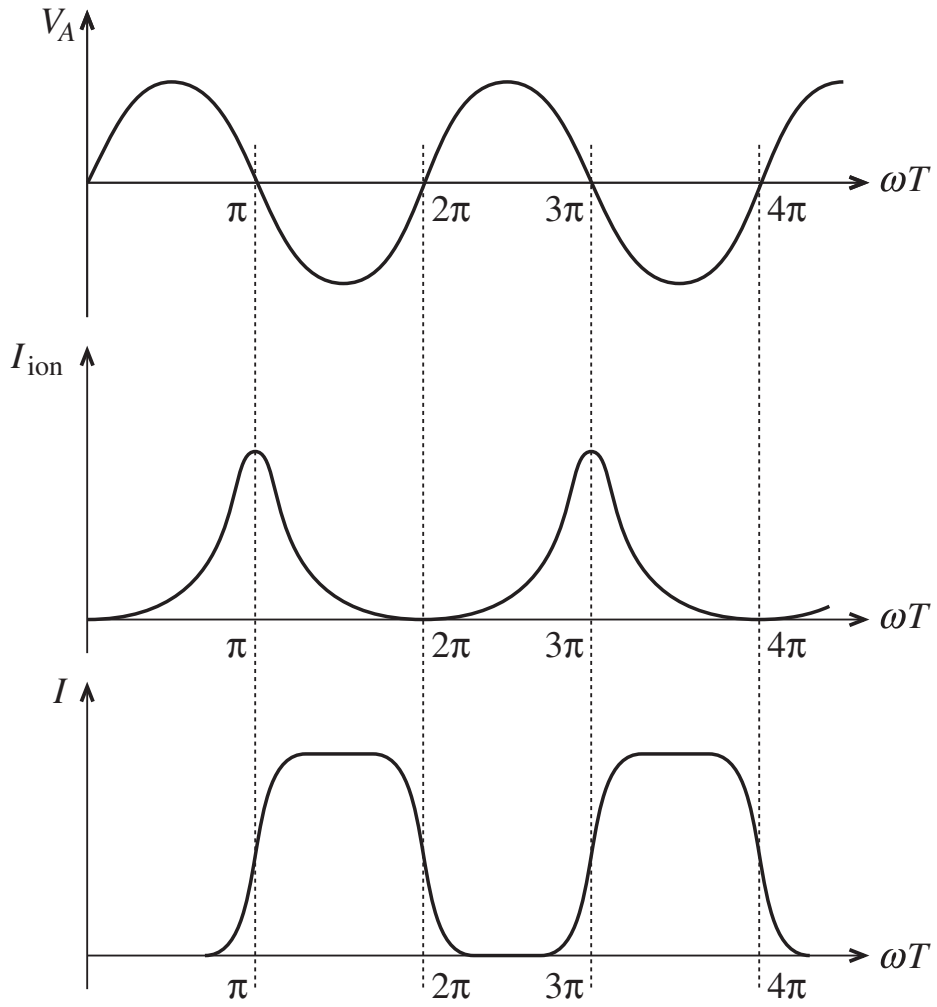


Figure 6-22 Applied voltage, ionization current, and total current of an IMPATT diode.

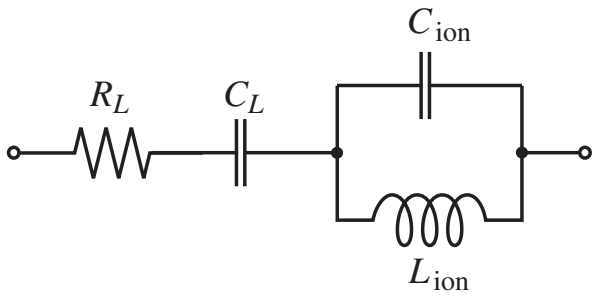


Figure 6-23 Electric circuit representation for the IMPATT diode.

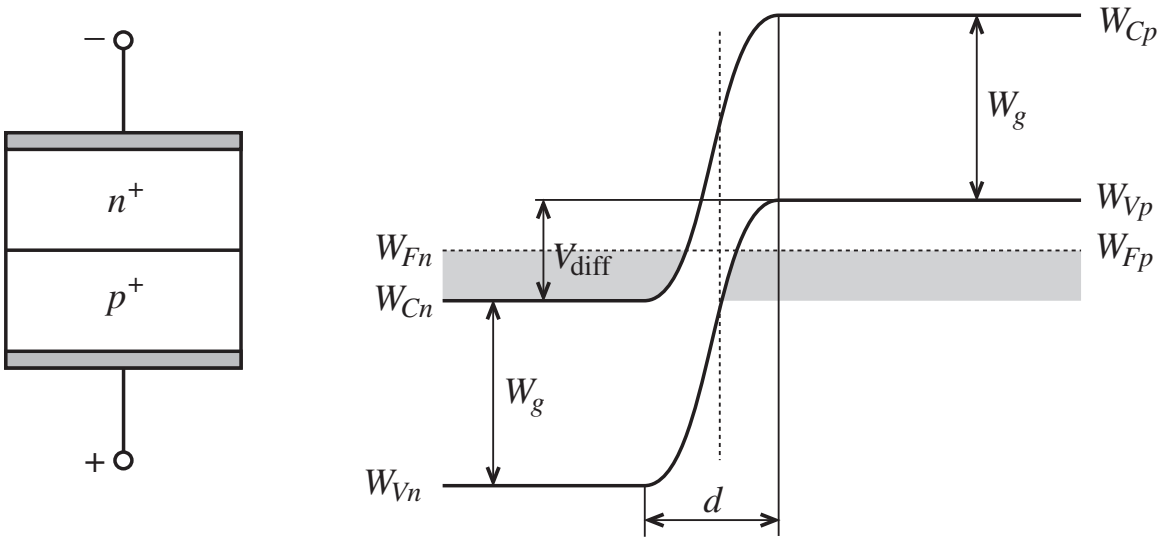
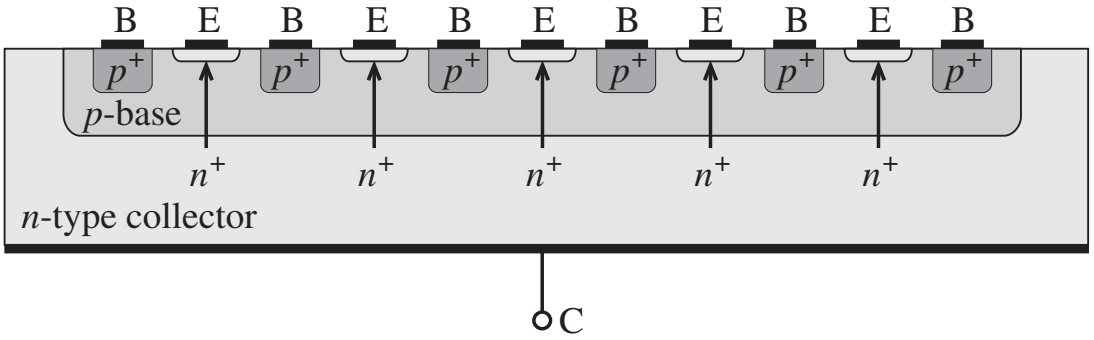
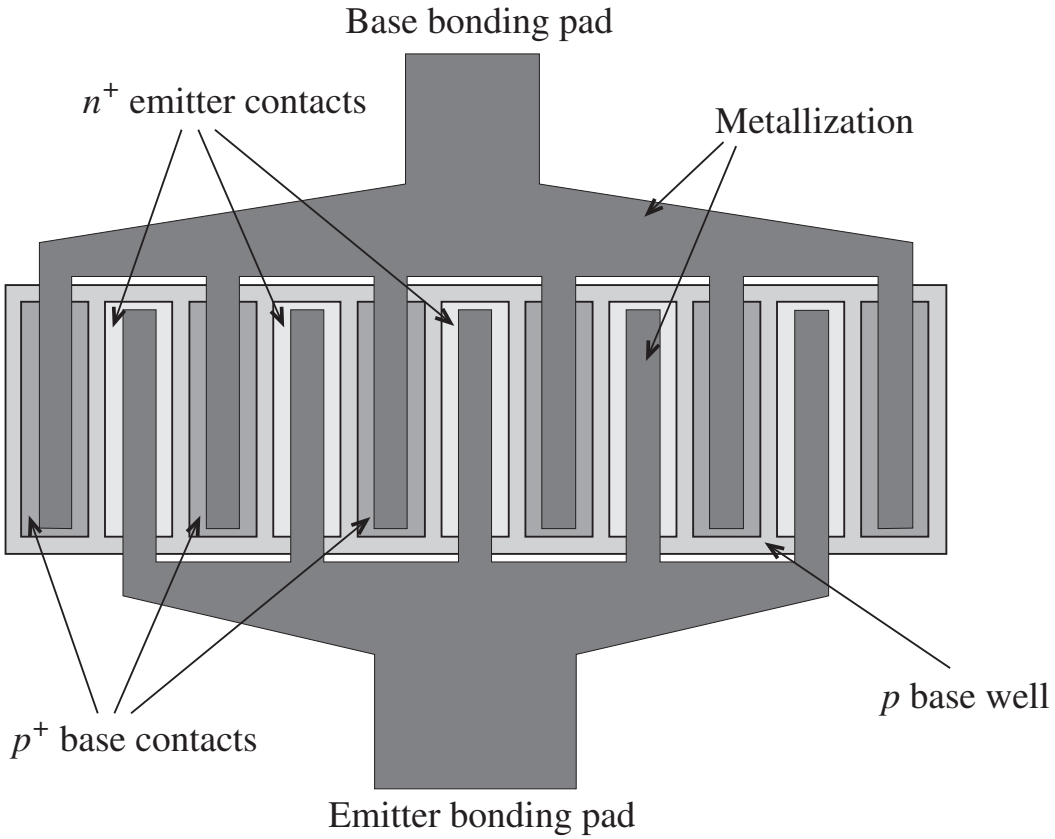


Figure 6-24 Tunnel diode and its band energy representation.



(a) Cross-sectional view of a multifinger bipolar junction transistor



(b) Top view of a multifinger bipolar junction transistor

Figure 6-25 Interdigitated structure of high-frequency BJT.

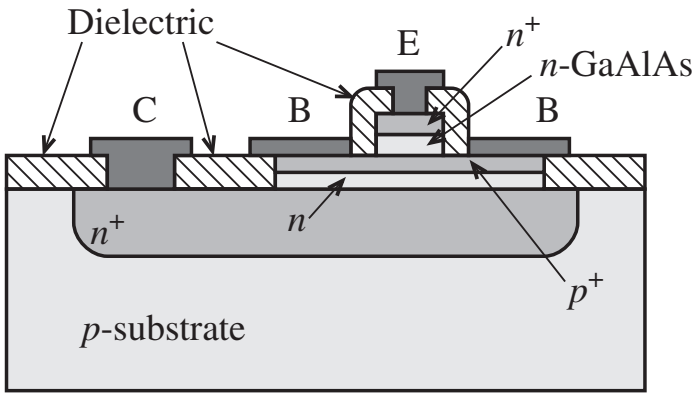


Figure 6-26 Cross-sectional view of a GaAs heterojunction bipolar transistor involving a GaAlAs-GaAs interface.

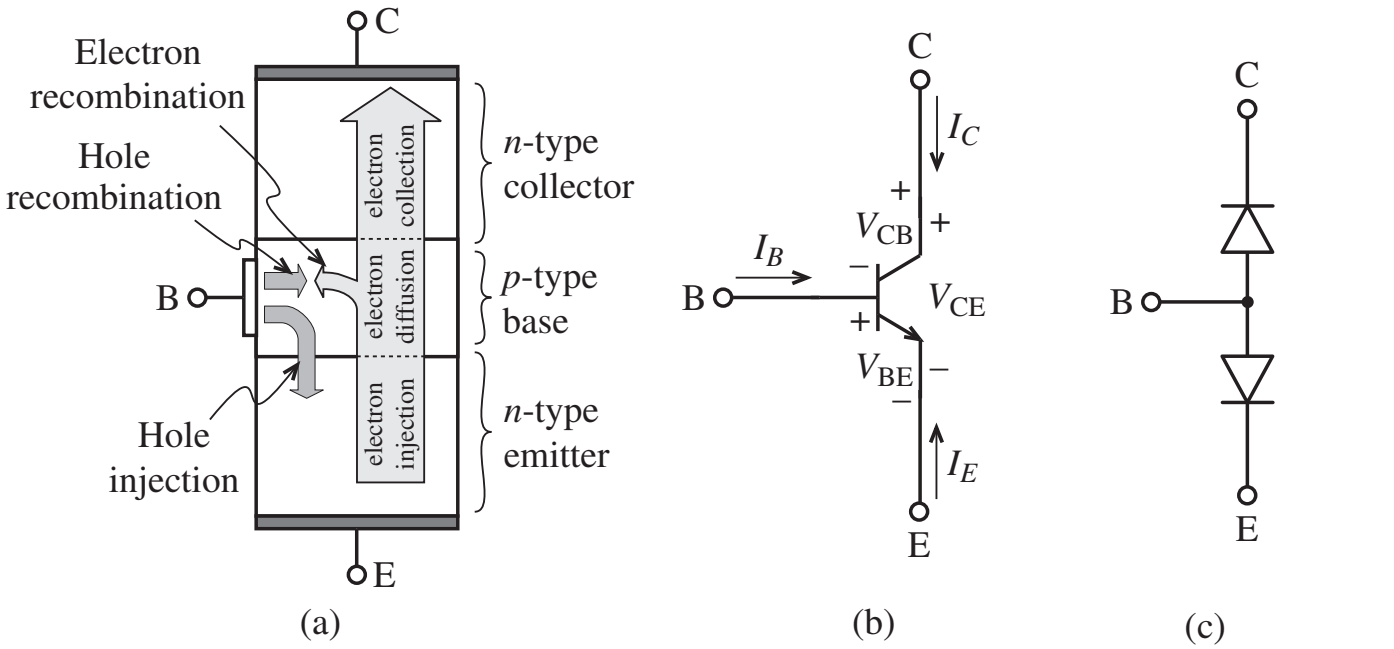
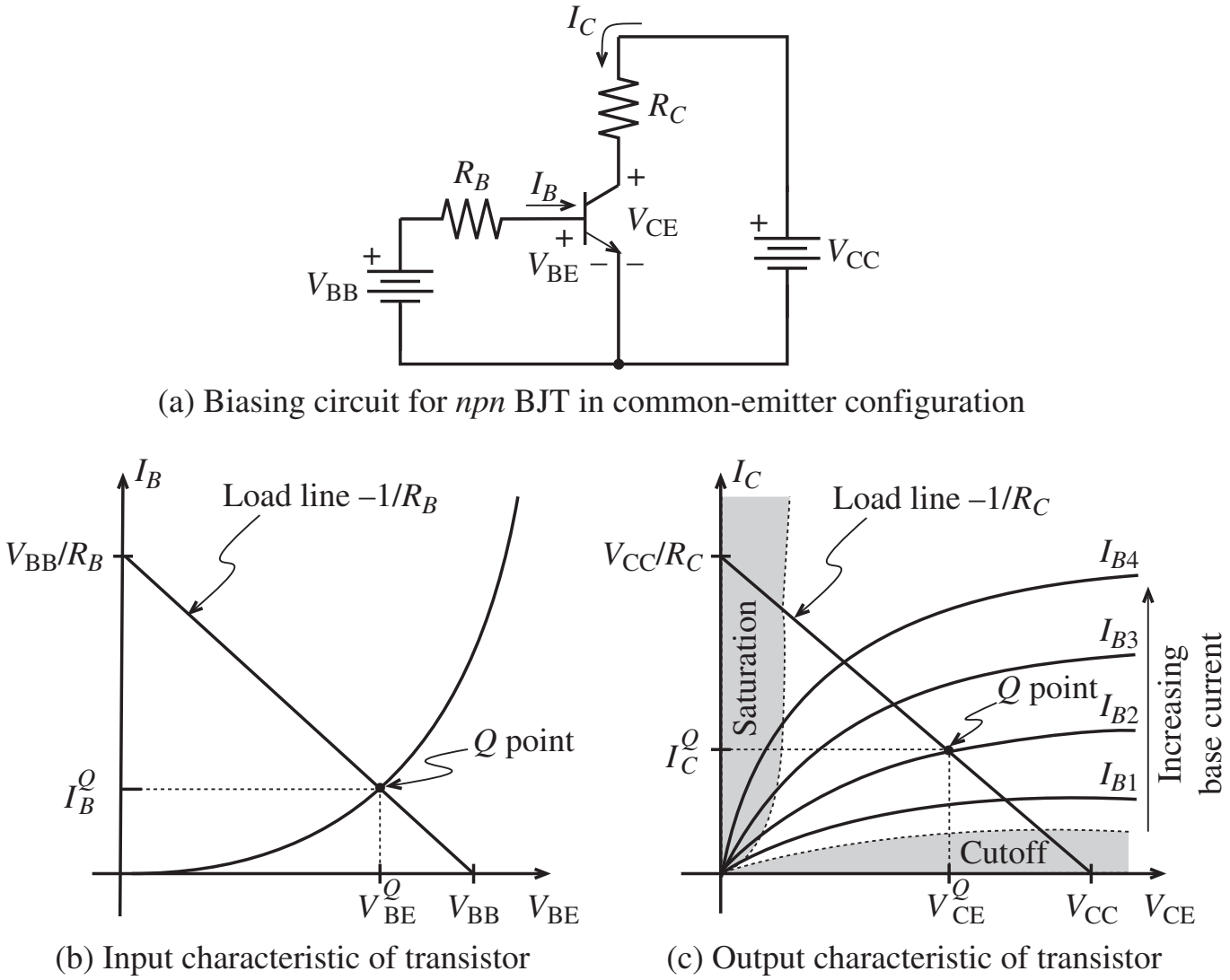


Figure 6-27 *npn* transistor: (a) structure with electrical charge flow under forward active mode of operation, (b) transistor symbol with voltage and current directions, and (c) diode model.



(a) Biasing circuit for *npn* BJT in common-emitter configuration

(b) Input characteristic of transistor

(c) Output characteristic of transistor

Figure 6-28 Biasing and input, output characteristics of an *npn* BJT.

Table 6-3 BJT parameter nomenclature

Parameter description	Emitter (*n*-type)	Base (*p*-type)	Collector (*n*-type)
Doping level	N_D^E	N_A^B	N_D^C
Minority carrier concentration in thermal equilibrium	$p_{n_0}^E = n_i^2 / N_D^E$	$n_{p_0}^B = n_i^2 / N_A^B$	$p_{n_0}^C = n_i^2 / N_D^C$
Majority carrier concentration in thermal equilibrium	$n_{n_0}^E$	$p_{p_0}^B$	$n_{n_0}^C$
Spatial extent	d_E	d_B	d_C

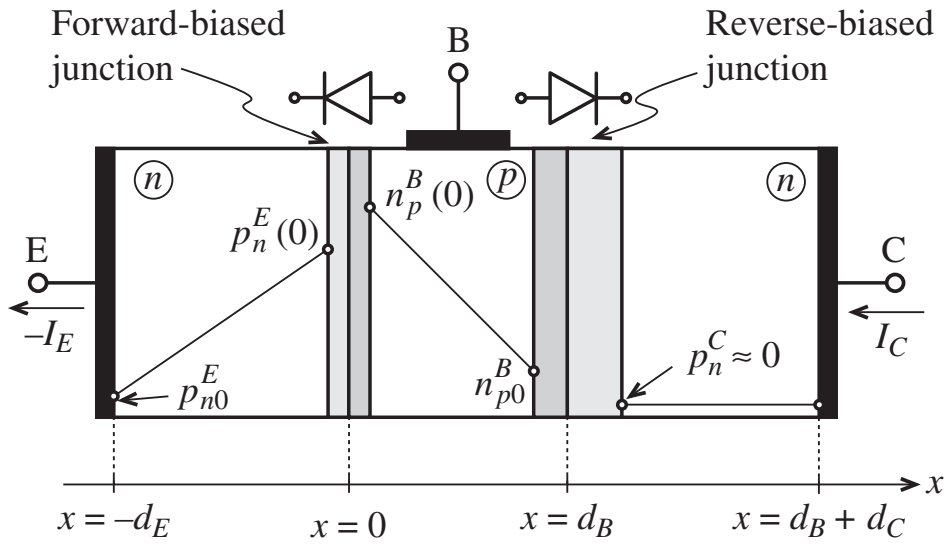


Figure 6-29 Minority carrier concentrations in forward active BJT.

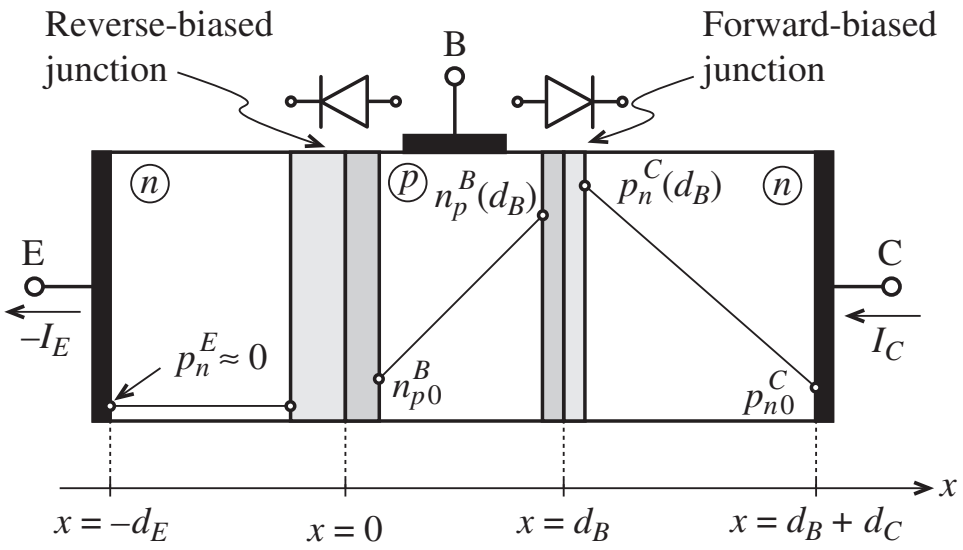


Figure 6-30 Reverse active mode of BJT.

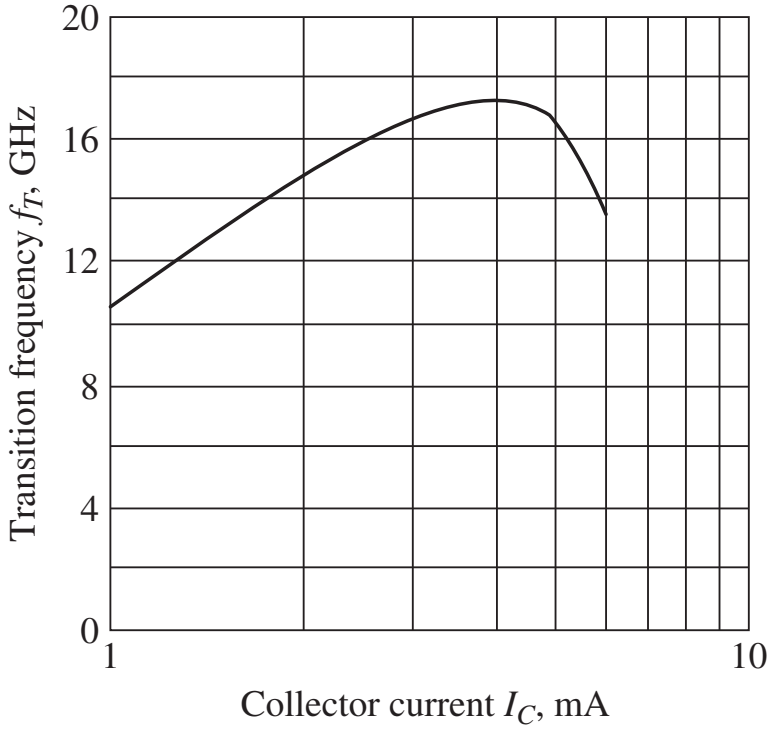


Figure 6-31 Transition frequency as a function of collector current for the 17 GHz *npn* wideband transistor BFG403W (courtesy of NXP).

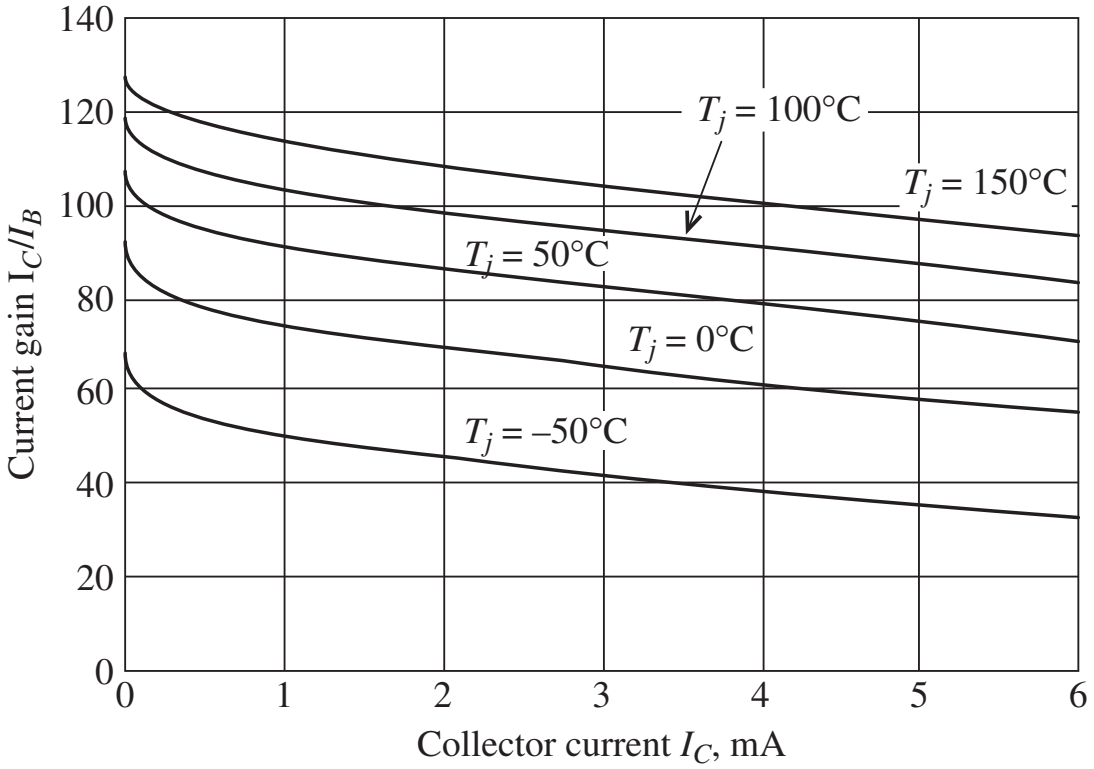


Figure 6-32 Typical current gain β_F as a function of collector current for various junction temperatures at a fixed V_{CE}.

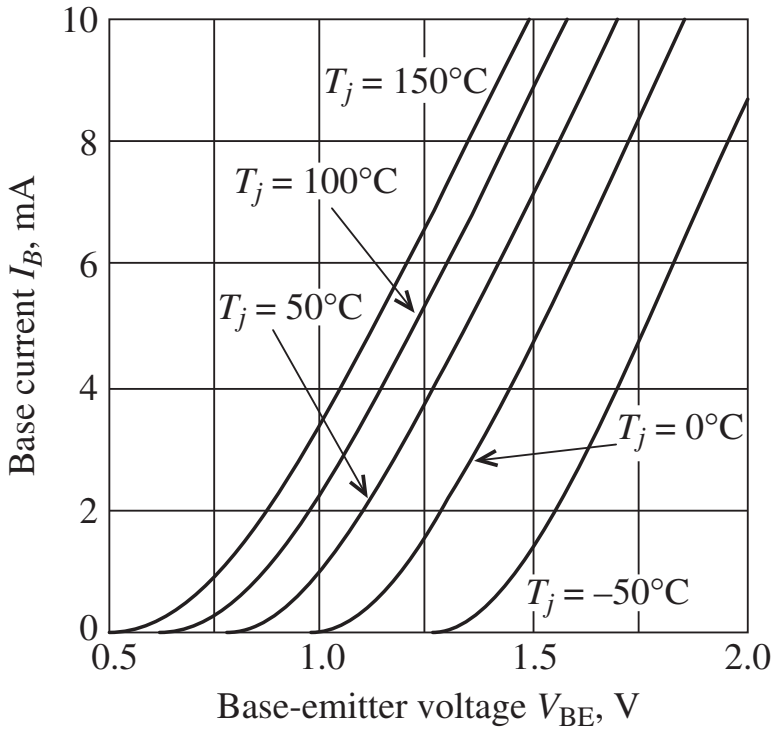


Figure 6-33 Typical base current as a function of base-emitter voltage for various junction temperatures at a fixed V_{CE}.

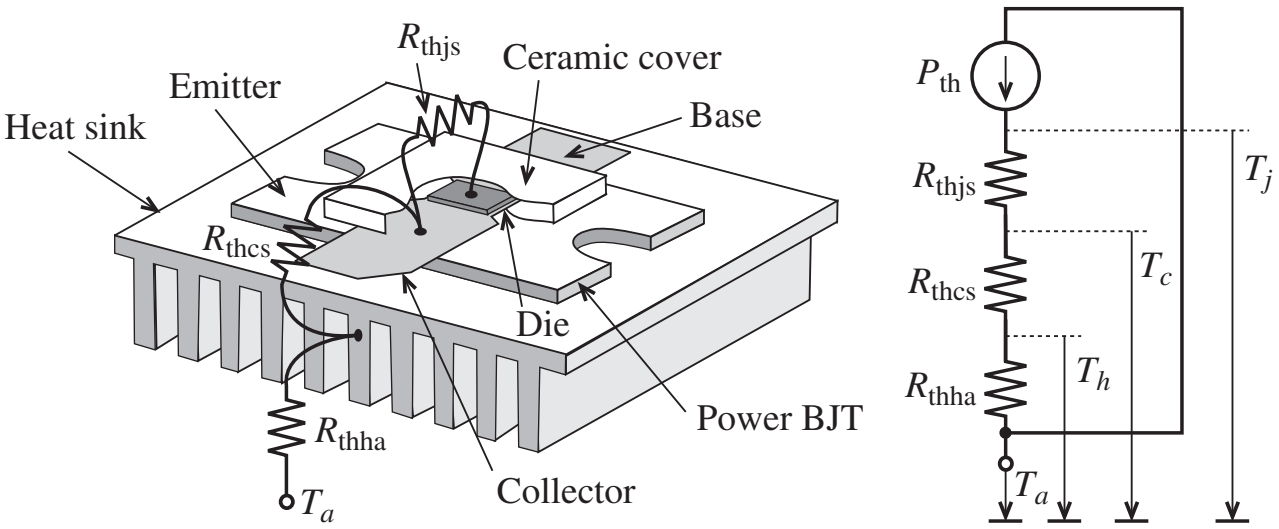


Figure 6-34 Thermal equivalent circuit of BJT.

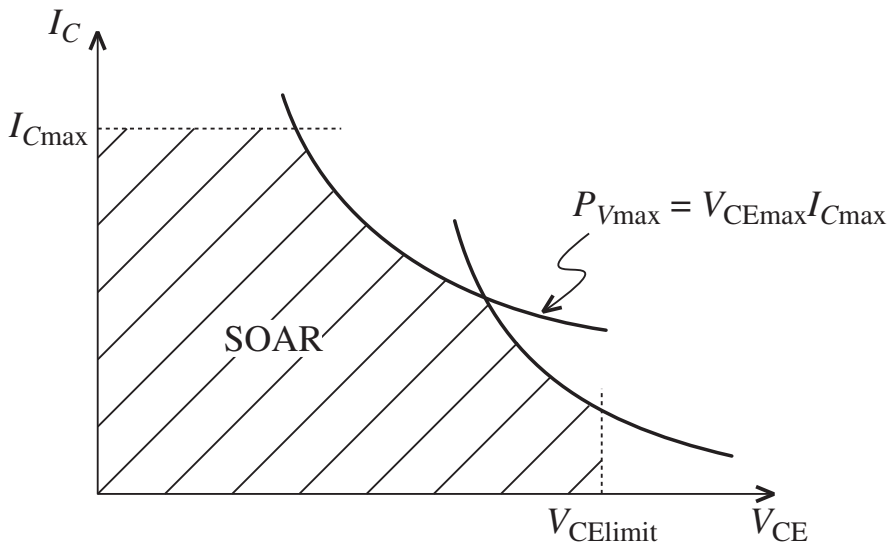
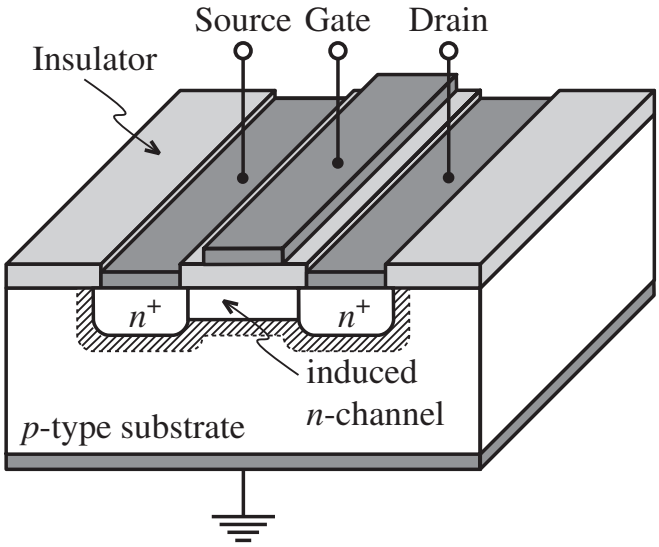
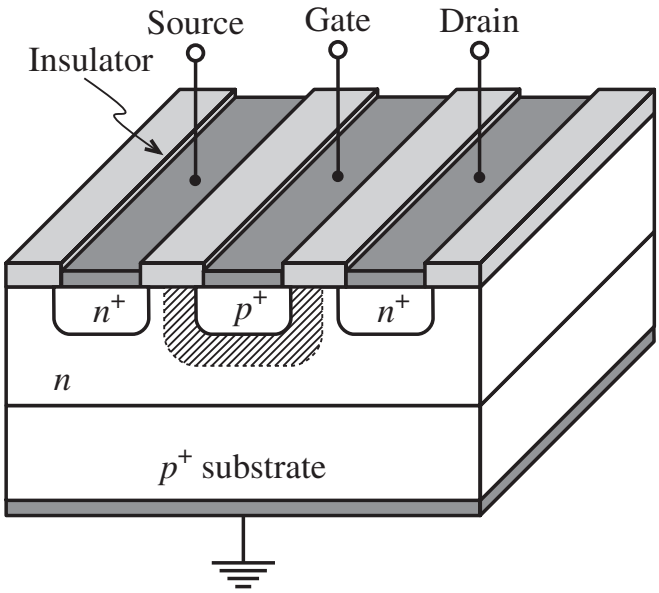


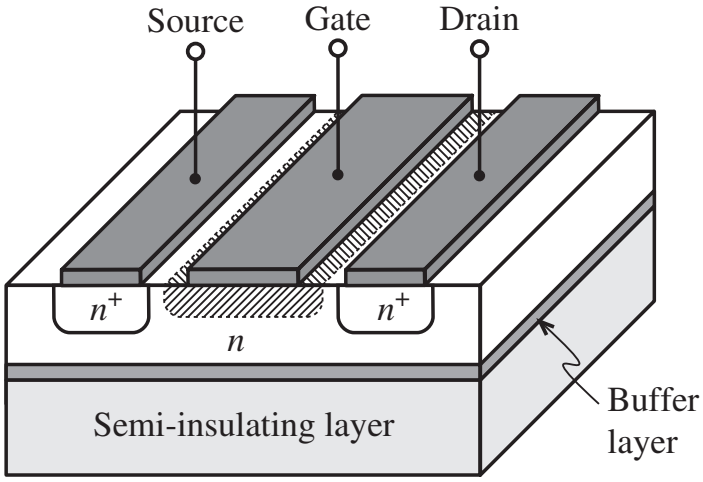
Figure 6-35 Operating domain of BJT in active mode with breakdown mechanisms.



(a) Metal insulator semiconductor FET (MISFET)

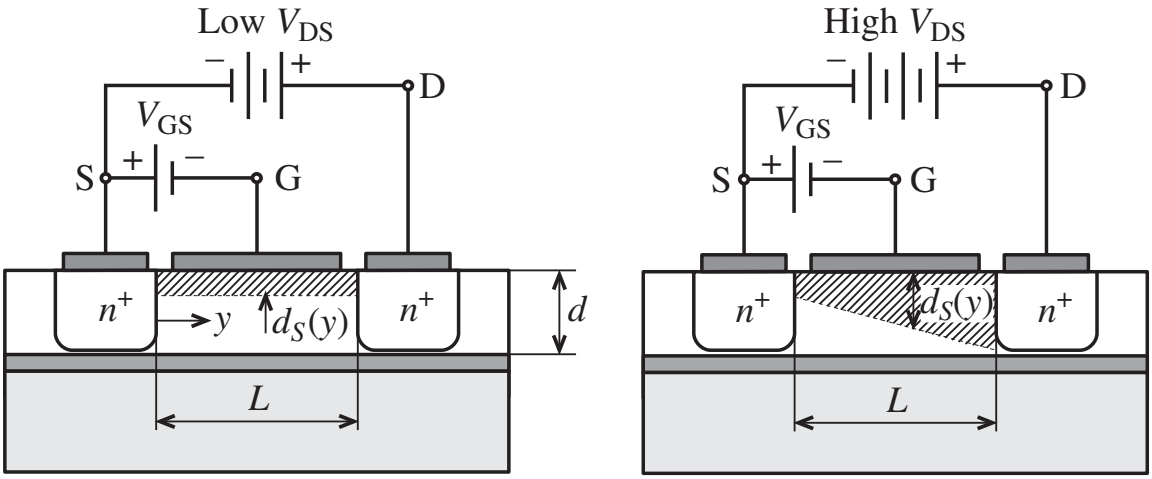


(b) Junction field effect transistor (JFET)



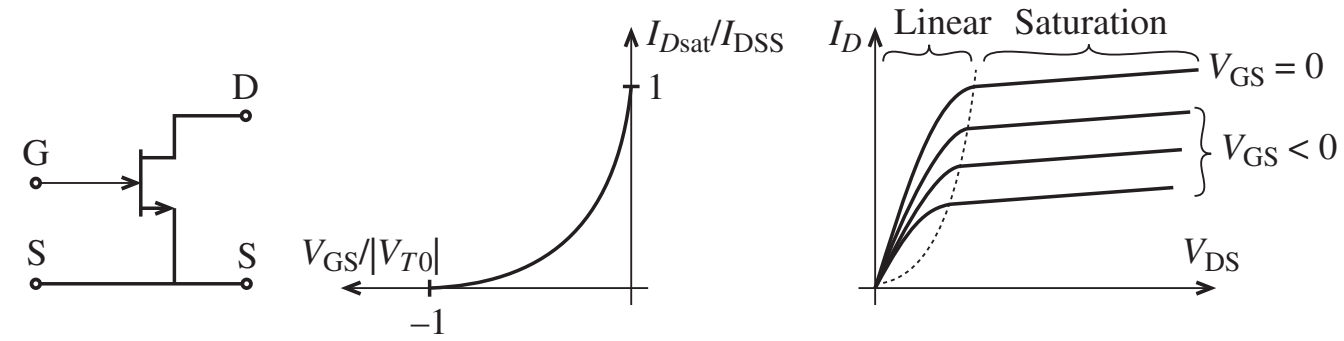
(c) Metal semiconductor FET (MESFET)

Figure 6-36 Construction of (a) MISFET, (b) JFET, and (c) MESFET. The shaded areas depict the space charge domains.



(a) Operation in the linear region. (b) Operation in the saturation region.

Figure 6-37 Functionality of MESFET for different drain-source voltages.



(a) Circuit symbol (b) Transfer characteristic (c) Output characteristic

Figure 6-38 Transfer and output characteristics of an *n*-channel MESFET.

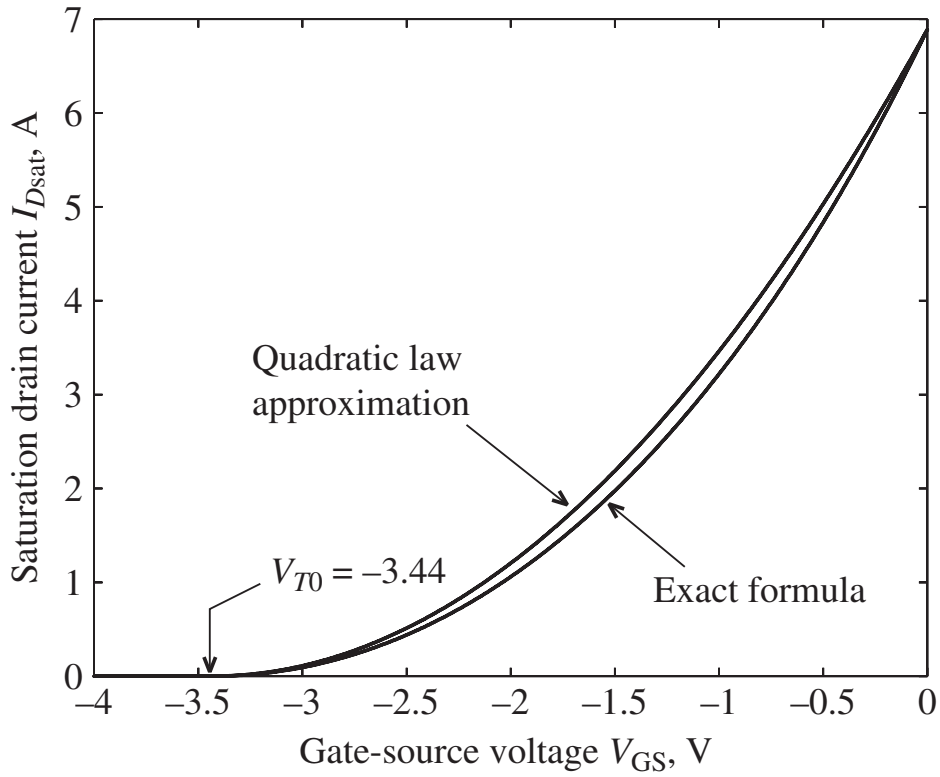


Figure 6-39 Drain current versus V_{GS} computed using the exact and the approximate equations (6.86) and (6.87).

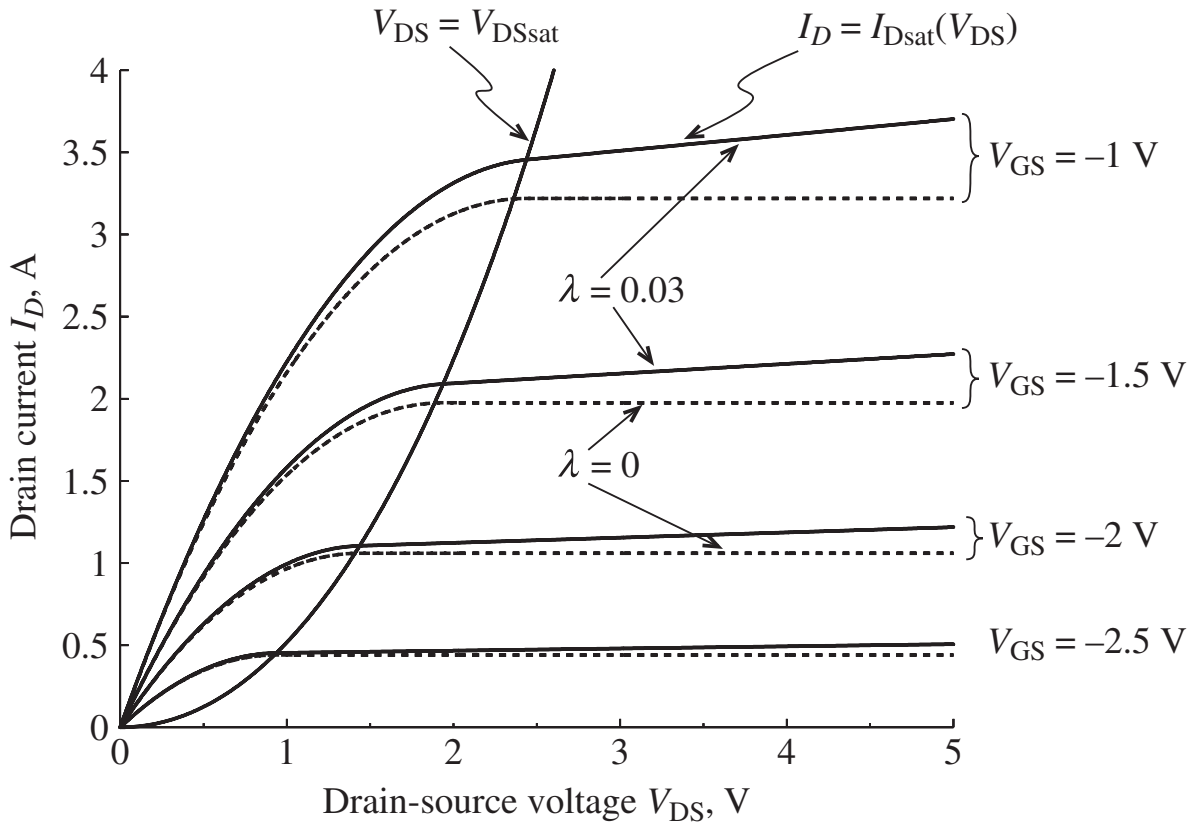


Figure 6-40 Drain current as a function of applied drain-source voltage for different gate-source biasing conditions.

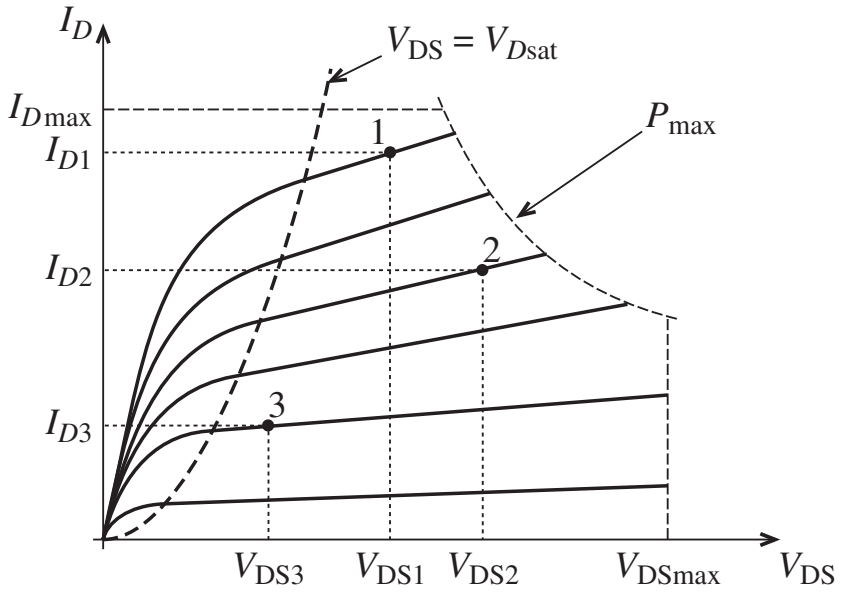


Figure 6-41 Typical maximum output characteristics and three operating points of MESFET.

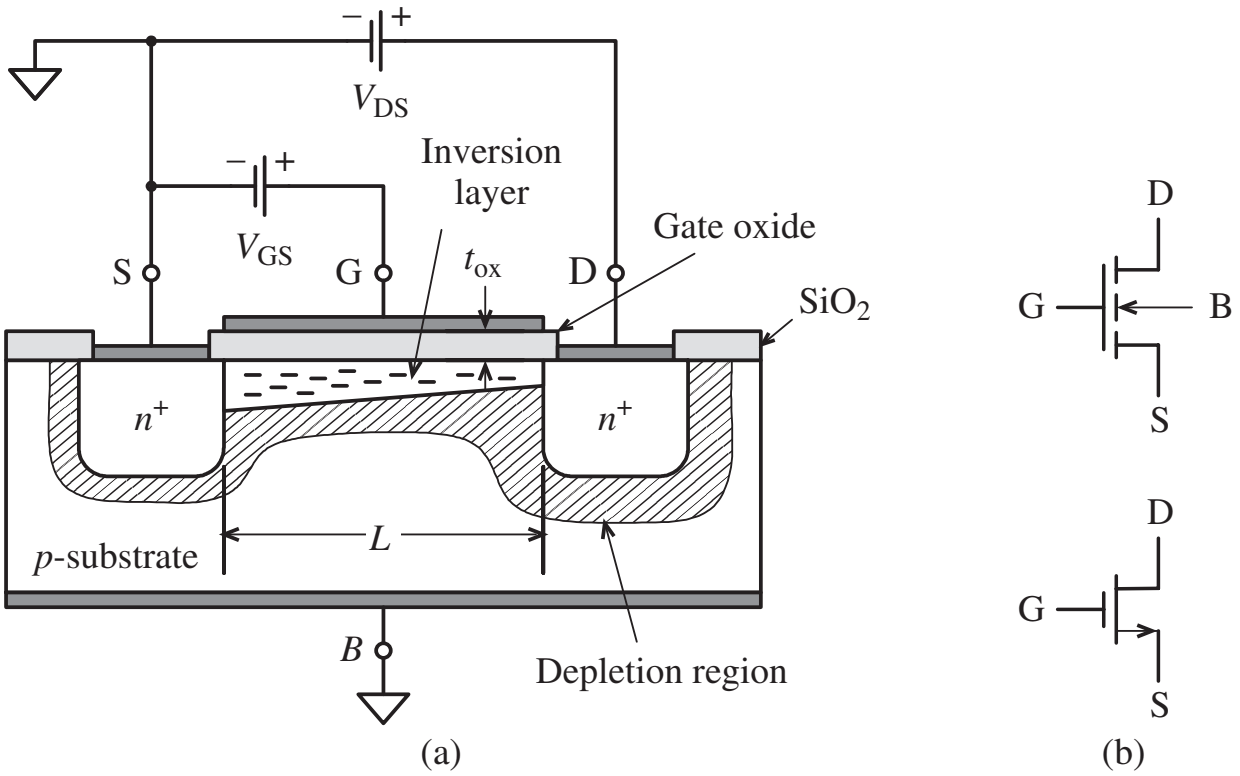


Figure 6-42 Cross-sectional view of an *n*-channel MOS transistor: (a) physical construction, (b) symbols.

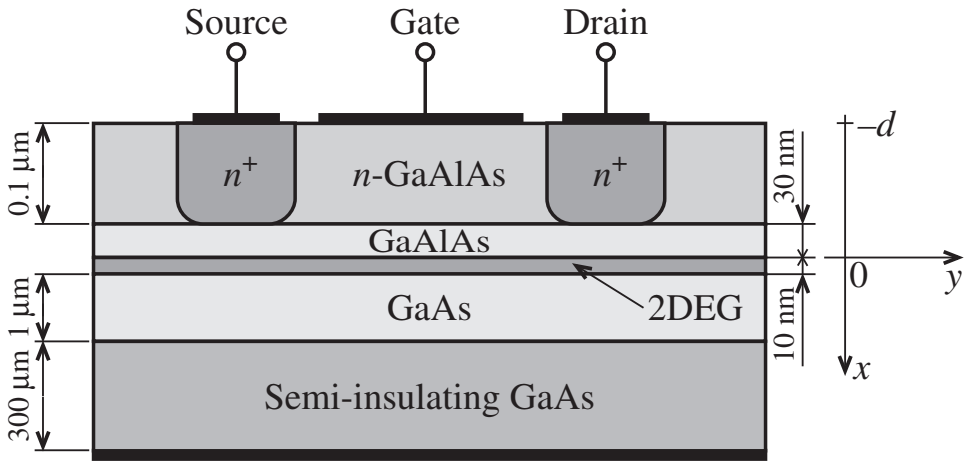
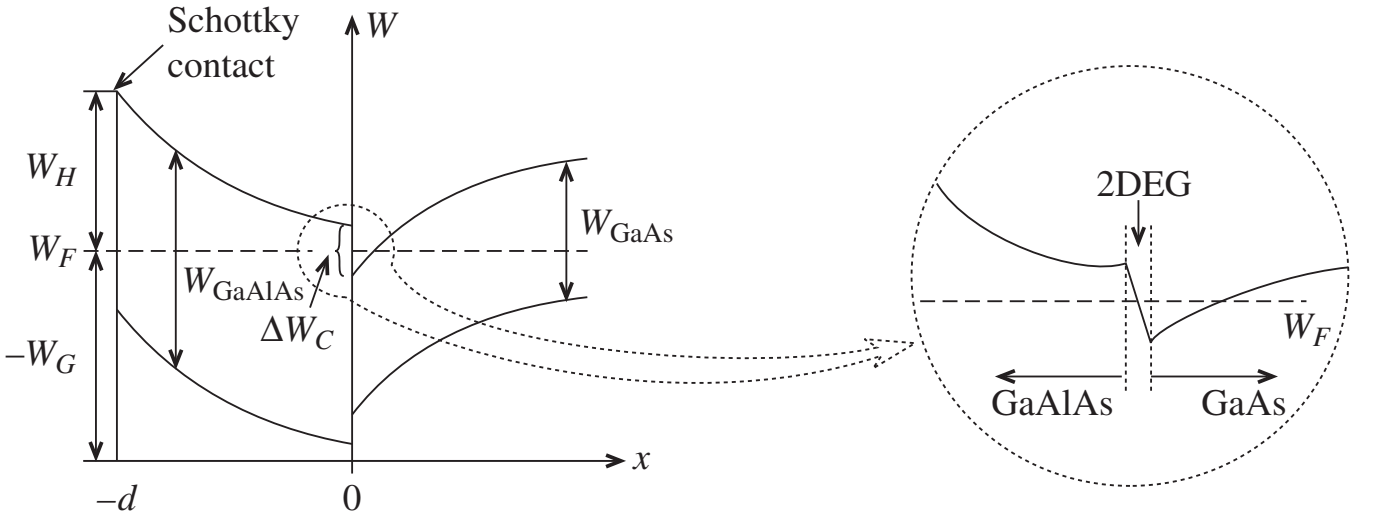


Figure 6-43 Generic heterostructure of a depletion-mode HEMT.



(a) Energy band diagram (b) Close-up view of conduction band

Figure 6-44 Energy band diagram of GaAlAs-GaAs interface for an HEMT.

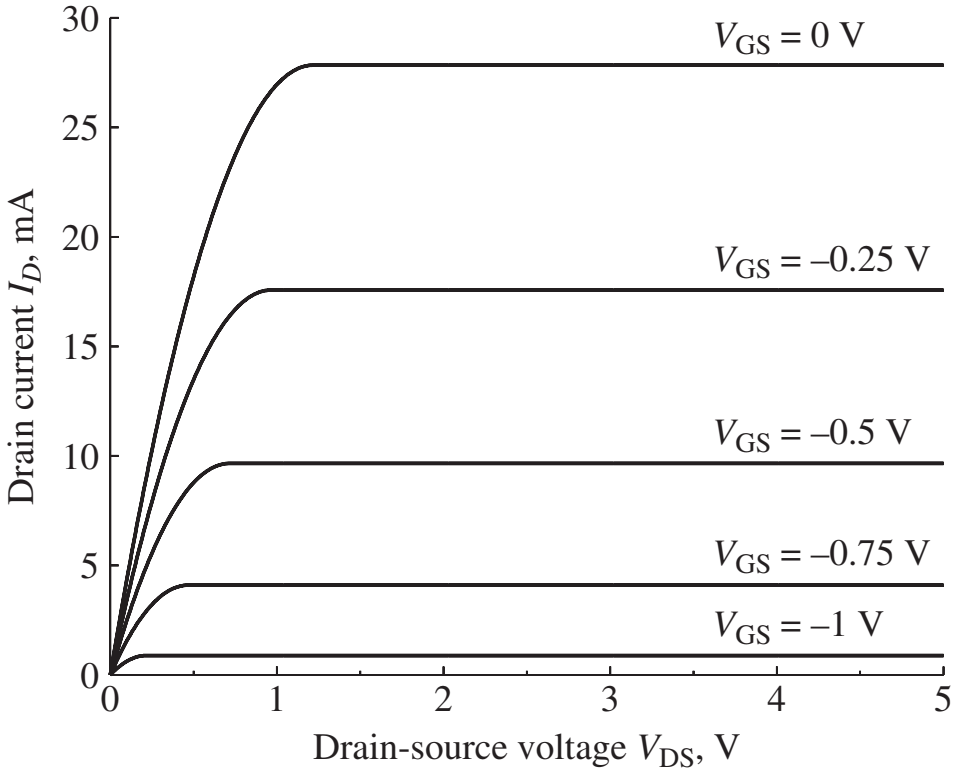
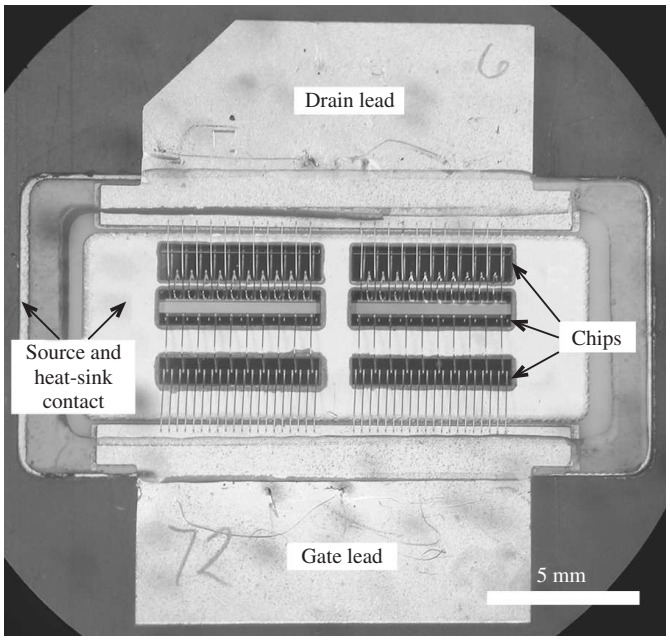
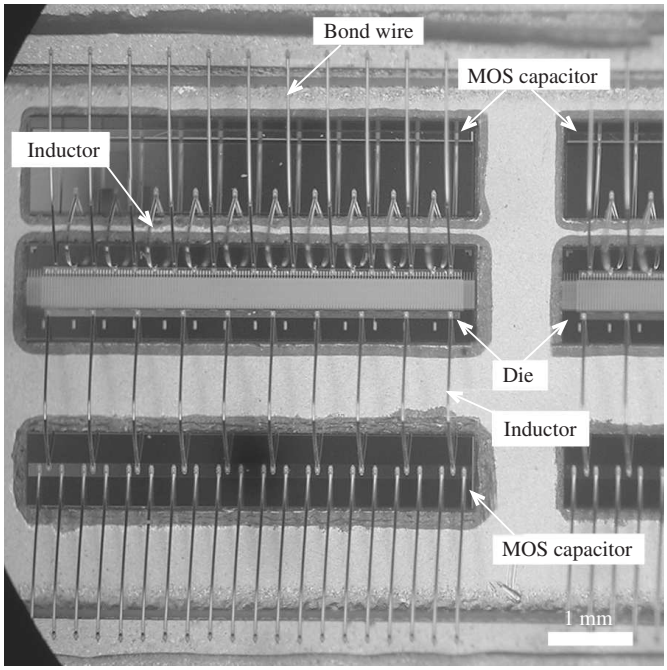


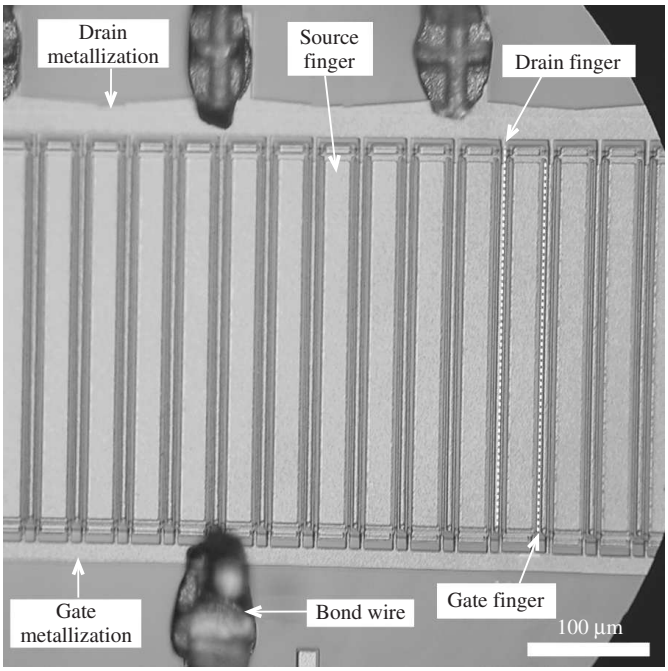
Figure 6-45 Drain current in a GaAs HEMT.



(a)



(b)



(c)

Figure 6-46 The internal structure of the LDMOS power transistor BLF4G22-100 at three levels of magnification: (a) overall package, (b) die interconnections, and (c) transistor die (courtesy of NXP).

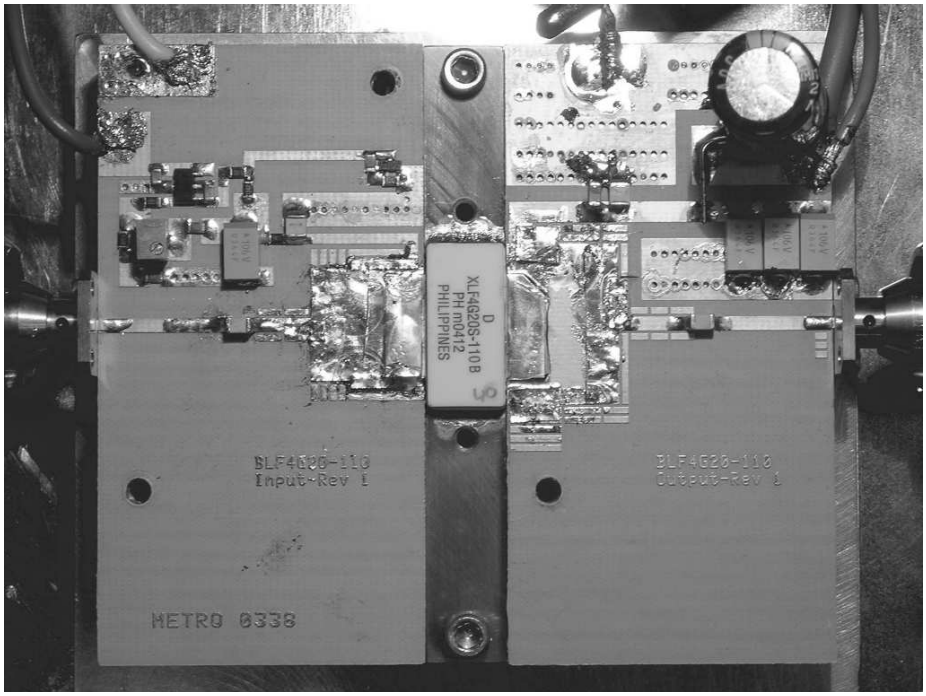


Figure 6-47 The power transistor mounted on a demonstration board.